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Common Channel Interoffice Signaling:

Technology and Hardware

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The CCIS hardware is a mix of electromechanical, discrete electronic, and new integrated electronic technologies blended together to allow economical conversion of No. 4A/ETS offices while at the same time matching the technology of the electronic toll offices in which it is incorporated. Connectorization and plug-in assemblies help achieve a design that can be readily maintained and administered.

I. INTRODUCTION

In the early development stages of this new signaling system the need for an integrated electronic technology approach for new units became apparent. A major new unit, the CCIS terminal, is required for the system operation in No. 4 ESS offices as well as in No. 1 ESS toll and in No. 4A/ETS offices. The thin film, beam leaded integrated electronic technology under development for the new No. 4 ESS design has been chosen for this equipment. Other units required in No. 4A/ETS offices only are based on Dual-In-Line Packages (DIP), printed circuit board and electromechanical elements more nearly matching the technology of that system.

This mix of hardware improves cost economies and takes advantage of manufacturing techniques already being employed by Western Electric. Using No. 4 ESS technology in the terminal design minimizes maintenance and administrative complexities in those offices. The design for No. 4A crossbar is optimized for conversion of offices by providing options for converting existing equipment rather than requiring the purchase of new frames.

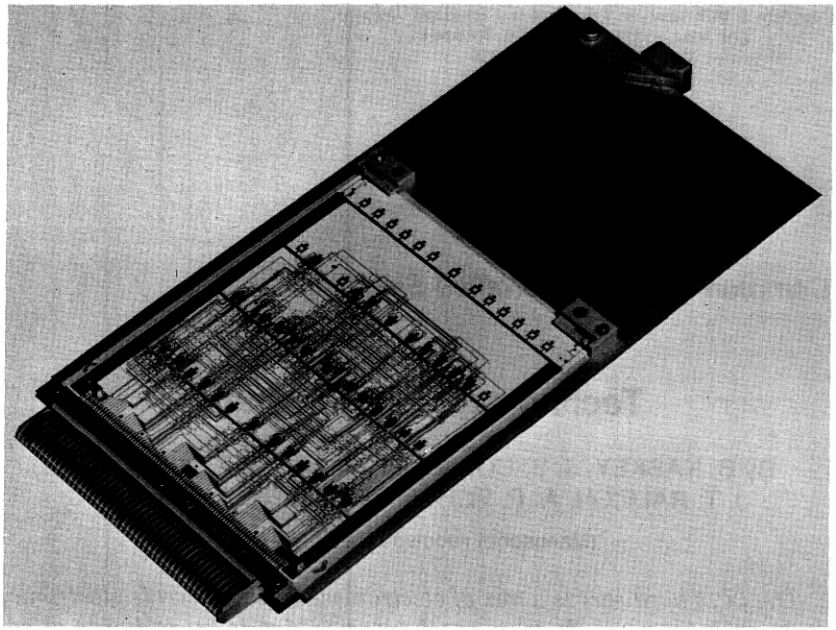

Fig. 1—Ceramic circuit pack.

II. APPARATUS AND HARDWARE TECHNOLOGY

2.1 Integrated electronic hardware

A new family of hardware, developed for use in No. 4 ESS, is used for CCIS equipment that resides in both No. 4A crossbar and No. 4 ESS offices. The hardware includes housings, connectors and circuit packs developed specifically for integrated circuit application. One type of circuit pack uses a unique ceramic carrier for mounting beam lead devices. The connector design assumes use of a rigid multilayer backplane for mechanical support and for distribution of power throughout each functional unit. The unit package is compatible with standard seven foot electronic frames.

The ceramic type of circuit pack which provides for logic circuitry is shown in Fig. 1. These packs place devices in predetermined locations. Connectivity between devices and to the attached connector is via conducting paths on the ceramic surface unique to each code. A system of computer programs generates the specific conducting array including crossover points for each circuit pack design. The back of each ceramic has a continuous ground plane primarily for shielding of the active devices and their connecting arrays. Ground shielding is also provided in the connector by a predetermined assignment of leads to ground via a connection at the ceramic. Circuit packs which use epoxy glass circuit

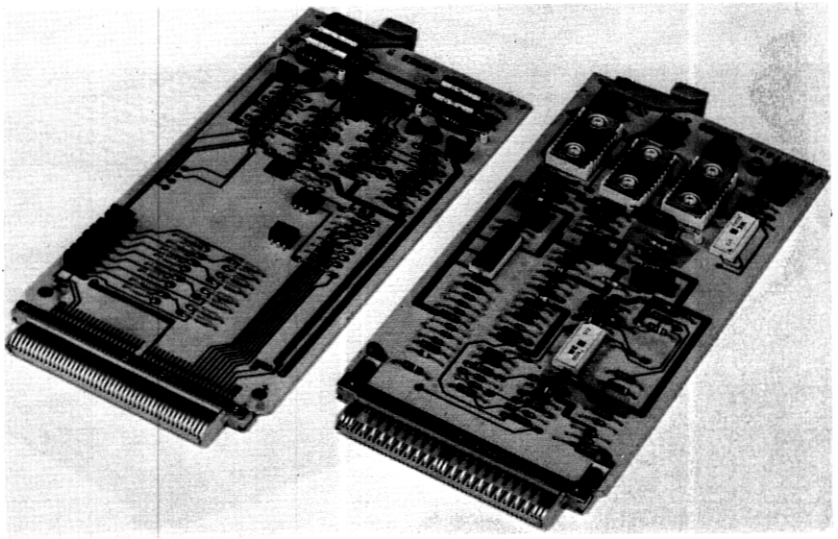

Fig. 2—Epoxy glass circuit pack.

boards and are employed for components other than beam lead devices are shown in Fig. 2.

The circuit pack housings are fabricated by forming sheet metal with ample open space to provide passages for air to aid in dissipating internal heat. These housings accommodate either 14 or 16 circuit packs.

Battery and ground are distributed across the unit by copper planes imbedded as layers in laminated multilayer backplanes. The insulating separators use an epoxy glass compound. Backplane designs are dependent upon each specific application. Connection from each layer is achieved by plated-through-holes which accommodate connector pins and have land areas on both outer surfaces of the backplane. The backplane forms an integral part of the unit mechanical structure as shown in Fig. 3. The pins of the connectors are inserted into the backplane and every pin of the connector is soldered to provide mechanical attachment and torsional support for the terminals. Each pin is individually removable to enhance repairability. Families of voltage converters, of the type shown in Fig. 4, have been designed for general use with this hardware. These converters use the office system voltage as input.

2.2 Dual-in-line integrated package hardware

The hardware system used for carrying dual-in-line integrated circuits is shown in Fig. 5. These packs are used to mount the Western Electric DIPs and other inline circuit components. The circuit pack is a double-

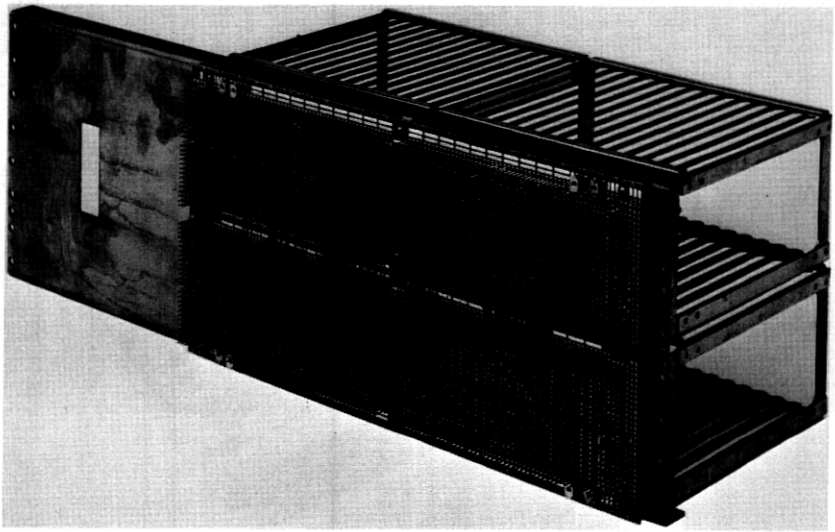

Fig. 3—Unit structure.

sided, epoxy glass board with plated through holes, gold plated fingers and is supplied with a card ejector. The connector which mates with this board has bifurcated contacts, used for ground, power, and signaling. The connector requires solderless wrap backplane wiring.

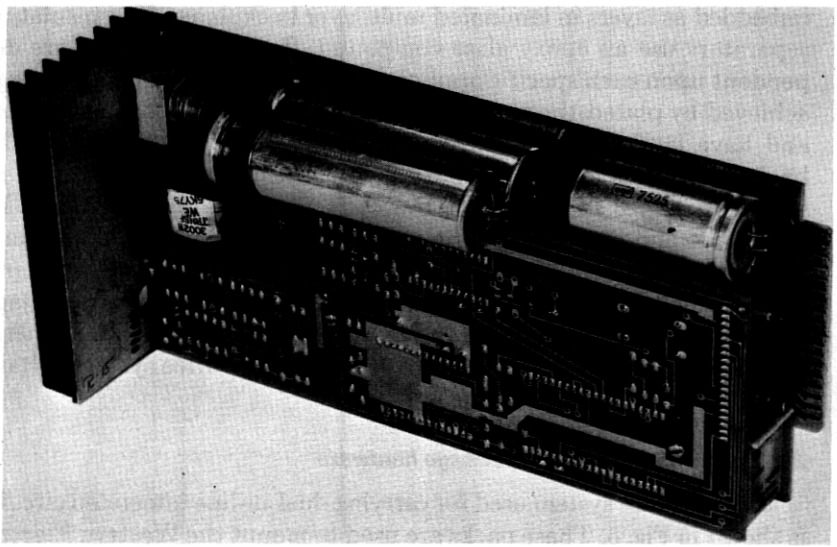

Fig. 4—Voltage converter.

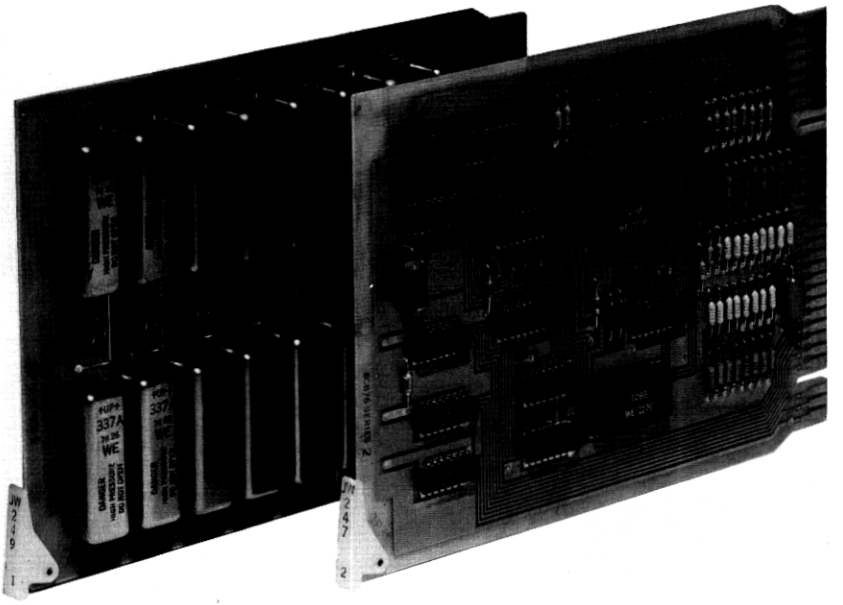

Fig. 5—Typical circuit packs for dual in-line packages and discrete components.

Two apparatus mountings for this type of circuit pack have been used, one for 11 packs and one for 16.

2.3 Discrete electronic and electromechanical hardware

Discrete electronic circuit packs are also used in combination with electromechanical hardware in the switching equipment area of the 4A crossbar machine. To accommodate this discrete electronic circuitry, circuit packs of the types shown in Fig. 6, have been designed.

Many new or modified functions are required in the existing portions of the 4A crossbar machine to provide CCIS capability. These are provided using existing electromechanical type hardware. Consequently many units are provided or modified using mounting plate units employing relays and switches with conventional solderless wrapped backplane wiring.

III. TERMINAL GROUP

The terminal group consists of equipment frames which contain CCIS terminals with associated Terminal Access Circuits (TAC). Separate configurations and TAC designs are provided to operate with No. 4A crossbar, No. 4 ESS and No. 1 ESS switching systems.

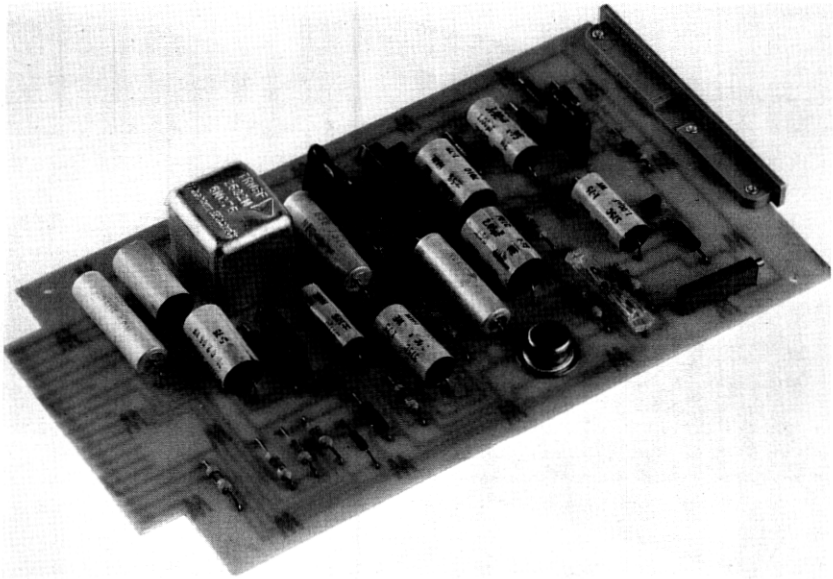

Fig. 6—Discrete component circuit pack.

3.1 No. 4A crossbar system terminal group

The specifications for the CCIS system define three basic functional blocks:

(*i*) A modem
(*ii*) A processor
(*iii*) A signaling terminal

The distribution of signaling functions between each functional block in a stored program control system is dependent upon the processor real time/peripheral hardware tradeoff.

Through the use of ESS 1A logic[1,2] and random access Insulated Gate Field Effect Transistor (IGFET) memory, the No. 4A CCIS terminal group implementation permits an extensive number of signaling functions to be assigned to the signaling terminal and modem at a reasonable cost.

A circuit not explicitly defined as part of the system specification is the Terminal Access Circuit (TAC). This circuit is tailored to the bus system of the host system central processor. Duplicated terminal access circuits interface the processor with up to 16 signaling terminal units.

The signaling terminal itself is a self-checking stored program controlled unit, with signal unit buffers realized by dynamically allocated linked-lists. This unit is common to the No. 4A and No. 4 ESS[3] CCIS systems.

A functional block diagram of the 4A terminal group is shown in Fig. 7. Each CCIS terminal unit is served by two TACs that provide a redundant path to the processor. Each terminal unit operates as a simplex unit and stores both outgoing signaling messages awaiting transmission and incoming messages until ready to be processed. The terminal unit also performs error control through redundant coding and retransmission of signaling messages found to be in error. Each terminal unit is dedicated to a modem that services one end of the signaling link. The modem forms a digital-analog interface between the terminal unit and the voice frequency link.

The CCIS terminal group consists of one CCIS terminal basic frame and two CCIS terminal supplementary frames. The terminal basic frame, shown in Fig. 8, is a 2-bay ESS frame. The frame mounts duplicated input-output and TAC units and up to six terminal units along with their associated fusing, power converters, and power control equipment. The input-output unit provides connectorized access to the SPC No. 1A processor busses. Terminal unit growth is facilitated by the use of connectorized flat-tape cables to connect the unit to the TACs.

Up to five additional terminal units can be mounted on each of two supplementary frames as shown in Fig. 9. Like the basic frame, fusing, power converters, and power control equipment associated with the terminal units are also mounted on the frame. Interconnections between the TAC units on the basic frame and terminal units on the supplementary frames are implemented with connectorized flat-tape cable.

Each terminal access circuit is capable of interfacing with Peripheral Unit Address Busses (PUAB) and with Scanner Answer Busses (SCAB) of the SPC No. 1A processor. Since all communication between the SPC No. 1A processor and the associated terminals is controlled by the TAC, the TAC must perform the following functions:

(*i*) Receive instruction and data from the central processor via the PUAB.
(*ii*) Check, decode, and analyze the information.
(*iii*) Select the sequence to be used.
(*iv*) Communicate the information to the proper terminal.
(*v*) Check the terminal response.
(*vi*) Transmit the requested data to the central processor via the SCAB.

Although duplicated, the TACs are operated in the simplex mode, with only one TAC active at a given time. The TAC is enabled via the Central Pulse Distributor (CPD). Since data or an operation code (opcode) can be communicated to either TAC over either PUAB, these enables are decoded by the TAC to determine the word type and the proper bus.

Commands from the processor either result in a terminal unit opera-

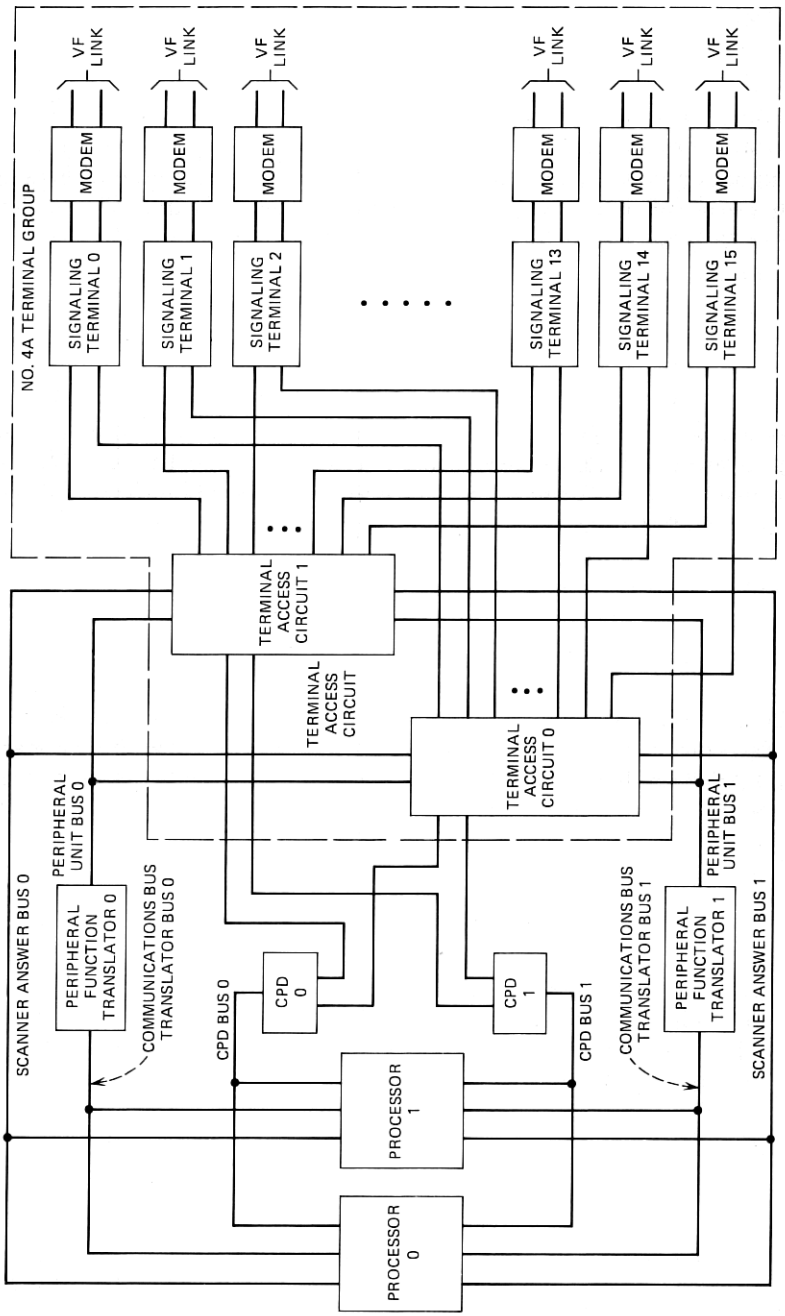

Fig. 7—No. 4A crossbar terminal group block diagram.

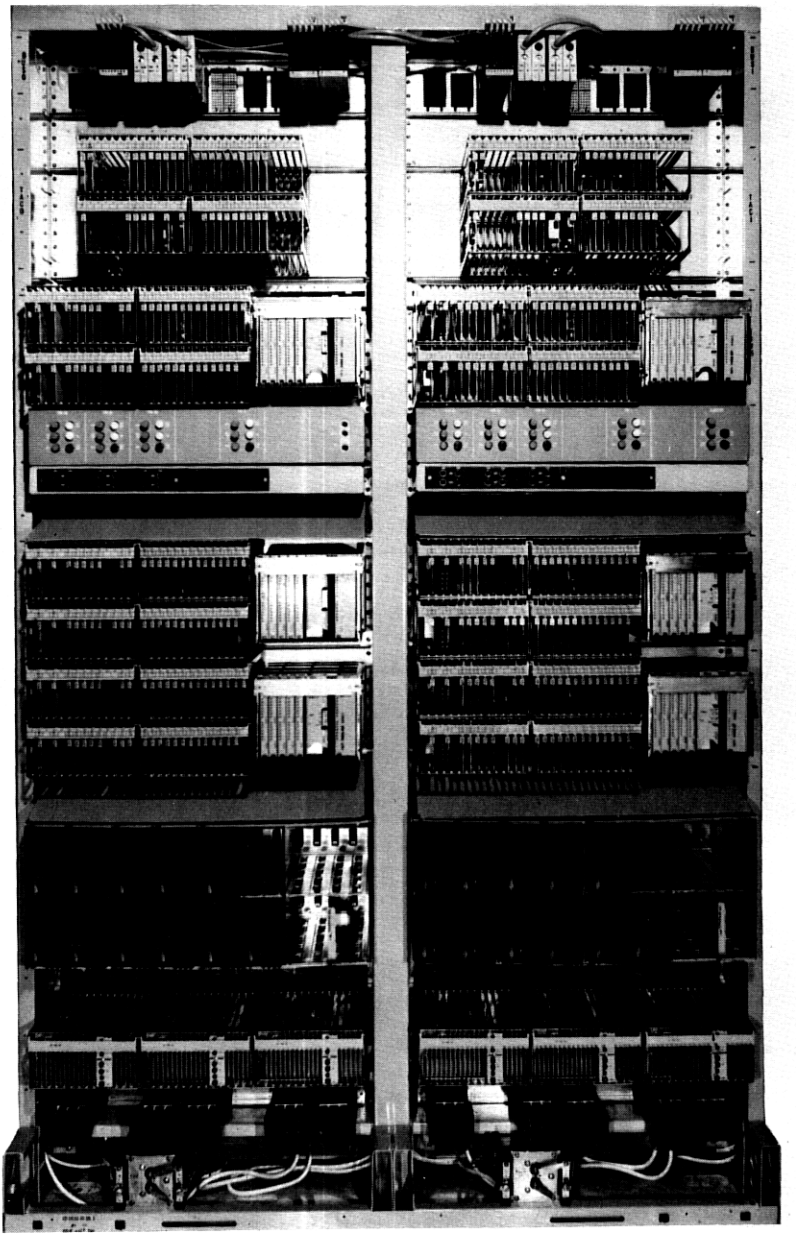

Fig. 8—4A terminal basic frame.

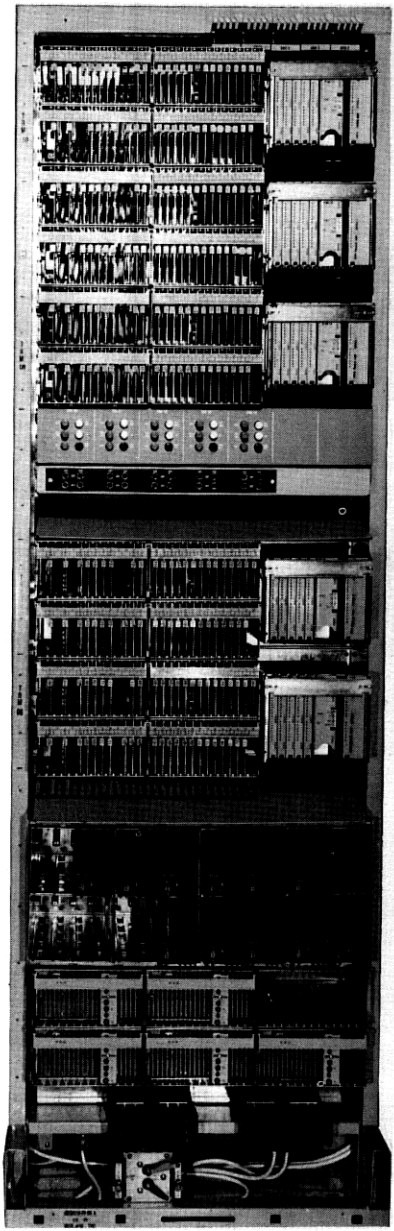

Fig. 9—4A terminal supplementary frame.

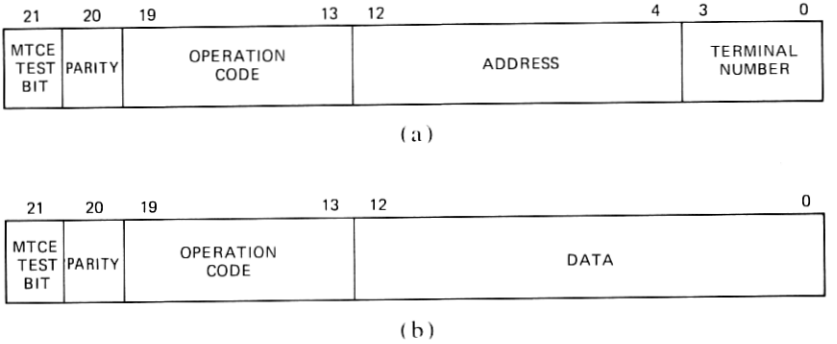

Fig. 10—(a) Terminal operation command format. (b) TAC operation command format.

tion or an internal TAC operation. The former commands are formatted as 20-bit words as shown in Fig. 10a. The opcode defines the task to be performed, the address specifies a particular register or memory location, and the terminal number indicates the terminal to be used. For TAC operations the instruction format is as shown in Fig. 10b. In this case, the data field contains information to be used during the task defined by the opcode.

The sequences initiated by the proper enabling of the TAC are controlled by a wired logic sequencer driven by a 12.5 MHz oscillator.

Communication with the terminal units takes place over two dedicated busses per terminal. Twenty-three bits of data plus a parity bit are transmitted over the 24-bit bidirectional TAC-To-Terminal (TTT) bus, and a 6-bit opcode plus a parity bit is communicated from the TAC to the terminal over the 7-bit Terminal Opcode bus (TOP). Additional leads are dedicated to each terminal for enable, all-seems-well, trouble, and buffer status signals.

The CCIS terminal unit is a small, self-contained, high-speed, stored program processor with an order structure tailored to CCIS operation. All signaling link related functions in the terminal unit are controlled by an internal stored program. The flexibility of this approach assures that the terminal can evolve with both the international and domestic signaling formats and can be compatible with data links using higher bit rates.

Figure 11 is a functional block diagram of the terminal unit. There are three separate control entities within the terminal. The Instruction Controller (IC) provides access to the program memory and executes the internally stored program. The Data Memory Controller (DMC) provides access to the data memory for both the internal stored program and the third controller, the I/O Controller (IOC). The latter handles all communications with the TAC. The three controllers operate asynchronously

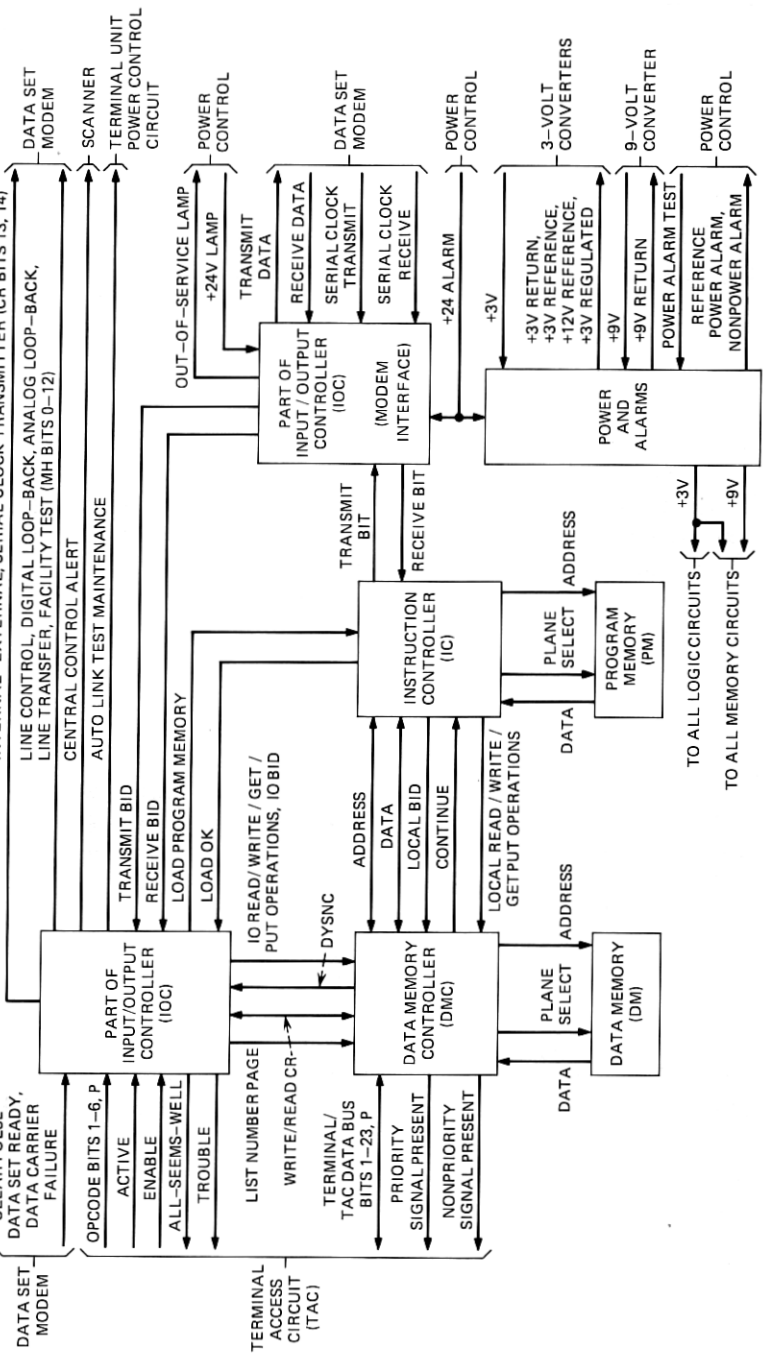

Fig. 11—Terminal unit block diagram.

with respect to each other and interact by requests, or bids, and acknowledgements. When one controller bids for service from another it waits until an acknowledgement is received before gating the data and removing the bid. The DMC can receive bids from both the IC and the IOC for access to the data memory. Both data and program memories are random access IGFET memories.

The instruction controller consists of an instruction sequencer, decoder, instruction address register and logic circuits used by the stored program. The set of instructions that can be executed by the IC are referred to as the internal order structure of the terminal and consist of logic, transfer, and memory access instructions.

A seven-phase instruction cycle is derived from a 12.5 MHz oscillator. The basic instruction cycle timing is shown in Fig. 12. As shown, the Instruction Address Register (IAR) is incremented during phase 1. Two phases are allowed for address propagation and plane select decoding prior to reading the memory. Phases 4, 5 and 6 allow for decoder and logic circuit settling times before loading internal registers. The sequencer is halted in phase 6 on bids to the DMC until the acknowledgement signal is received from the DMC. The sequencer can also be halted on command from the processor and is halted automatically upon detection of an error which affects normal terminal operation.

The program memory can be equipped with up to sixteen 128-word modules, or planes. The output of the program memory drives the instruction decoder directly, where the opcode is decoded along with various parameters to be used in the programmed operation.

All logic operations under control of the internal stored program involve the use of a 23-bit Logic Register (LR). The functions associated with the LR include rotation, masked insertion, incrementation, check code generation, and interface with the modem. Referring to Fig. 13, generation of an 8-bit check code is performed by executing a 1-bit rotation with the cyclic check code feedback logic enabled. For transmission, the contents of LR bit one is gated to the modem interface and the LR is rotated one bit to the left. Likewise, for receiving serial data from the modem, the LR is rotated one bit and the current receive bit from the modem interface is gated into LR bit nine.

The internal order structure of the terminal unit is tailored to the performance of CCIS signaling functions. The instruction repertoire is summarized in Fig. 14.

Of the 12 bits per program word, the first three to six bits are used for the opcode, the twelfth bit is a parity bit, and the remaining bits are used for option and parameter fields. All instruction addressing is direct and program flow is sequential, except where altered by transfer operations.

Access to data memory is provided by the DMC. The DMC can receive

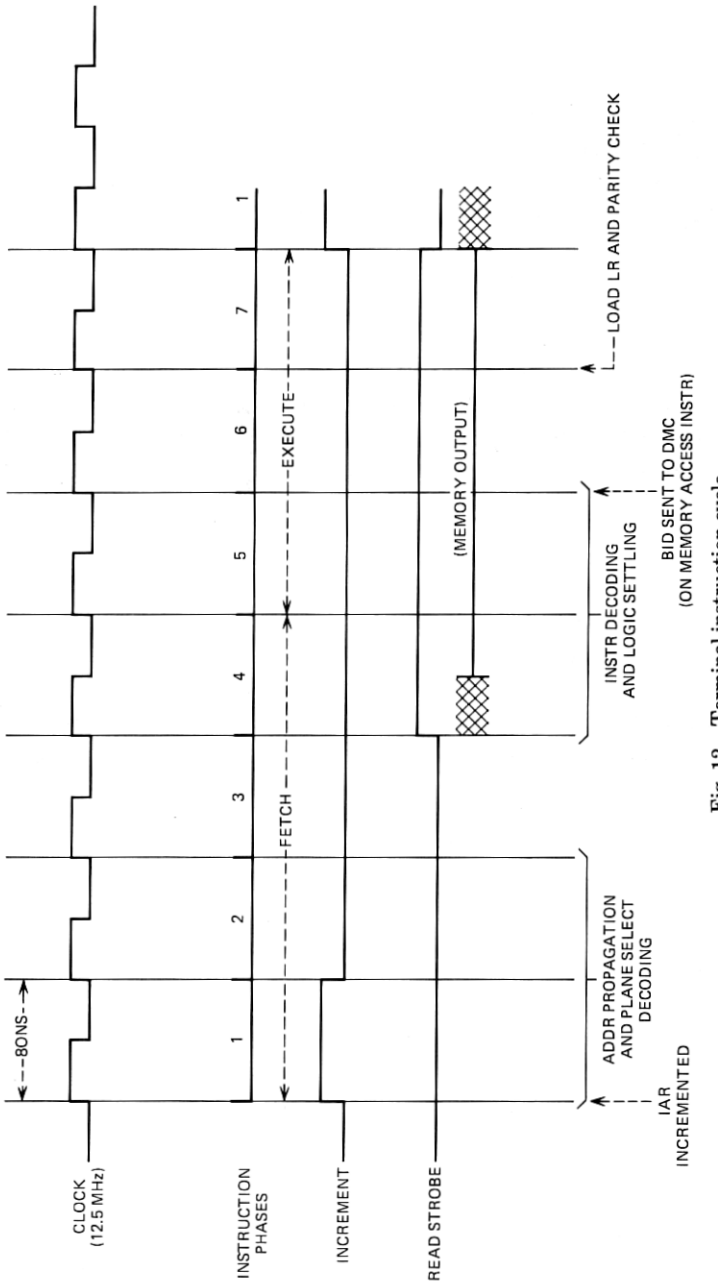

Fig. 12—Terminal instruction cycle.

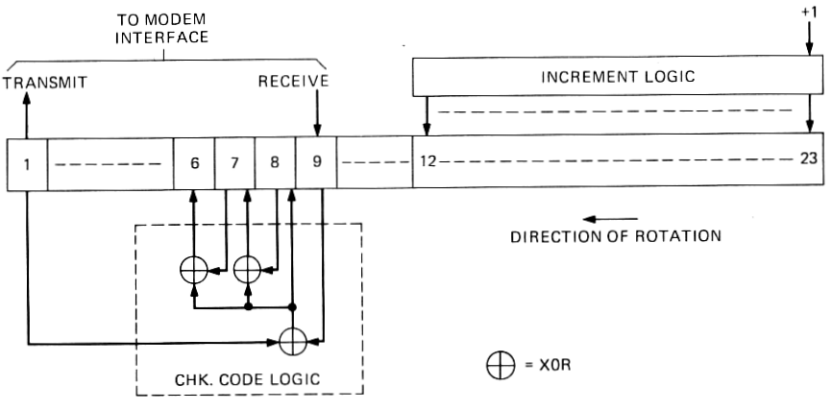

Fig. 13—Logic register layout and check code generation.

INSTRUCTION	DESCRIPTION
MOVE	COPIES CONTENTS OF REGISTER RI INTO REGISTER R2
ROTATE	CAUSES ENTIRE CONTENTS OF LOGIC REGISTER TO BE ROTATED (WITH END–AROUND CARRY) TO THE LEFT N BITS
INCREMENT	ADDS ONE TO THE CONTENTS OF THE LOGIC REGISTER
LOAD	INSERTS A FIELD OF DATA INTO THE LOGIC REGISTER WITHOUT DISTURBING THE REMAINING BITS
TEST BIT	TESTS THE VALUE OF A PARTICULAR BIT IN THE LOGIC REGISTER
TEST BYTE	TESTS A FIELD OF BITS IN THE LOGIC REGISTER
TEST DIRECT	COMPARES A FIELD OF BITS IN THE LOGIC REGISTER WITH A CONSTANT STORED IN THE INSTRUCTION
READ	READS A 23–BIT WORD OUT OF DATA MEMORY
WRITE	WRITES A 23–BIT WORD INTO DATA MEMORY
READ CR	MOVES THE CONTENTS OF THE CONTROL REGISTER INTO THE LOGIC REGISTER AND LEAVES THE CONTROL REGISTER UNCHANGED
WRITE CR	WRITES ONE OR MORE BITS IN THE CONTROL REGISTER
GET	RETRIEVES A 23–BIT ITEM FROM A SPECIFIED LIST
PUT	PLACES AN ITEM ON A SPECIFIED LIST

Fig. 14—Terminal unit internal instruction set.

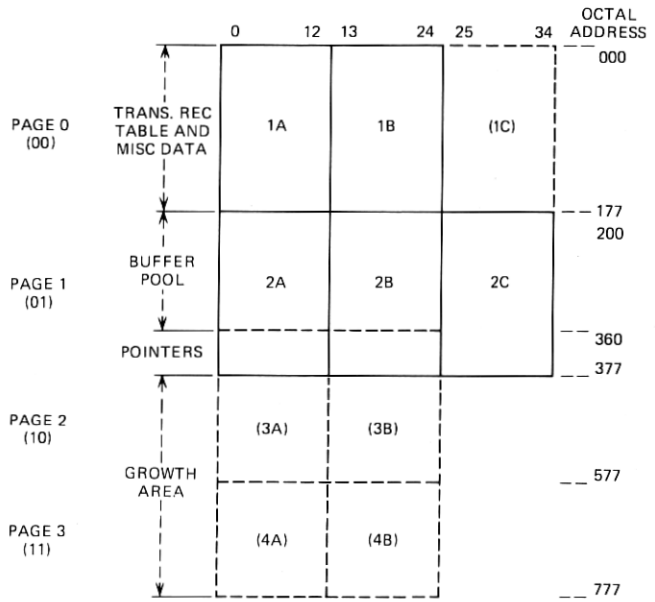

Fig. 15—Data memory organization.

service requests from both the instruction controller and the I/O controller. As a result of these bids, the DMC generates the memory address, selects the data path to or from the memory, administers the signal unit buffers, and provides the necessary memory timing sequence. A common 12.5 MHz oscillator is used to drive the DMC and the IC.

Data memory, independent of program memory, is provided for receive and transmit buffers, buffer pointers, and the transmit record table, as well as for miscellaneous data required by the internal program. The organization of the data memory is shown in Fig. 15. As shown, the memory is divided into four pages, denoted 0, 1, 2, and 3, each page having as many as three sections, denoted A, B, and C. Each section is implemented with a 128-word IGFET memory plane, identical to that which is used in the program memory. Unlike program memory, however, data words may be 24 or 34 bits in length. The longer word length is used for the receive and transmit buffer area, and typically consists of a 20-bit signal unit, an 8-bit link forward pointer which gives the location of the next item in the buffer, and various parity bits.

Receive and transmit signal unit buffers are realized by "first-in, first-out" linked-lists, 16 of which can exist simultaneously in the buffer area of data memory. Each of the 16 lists has associated with it a word in memory which contains a first-in pointer and a last-in pointer, specifying the location of the first-in and last-in items on that list, respec-

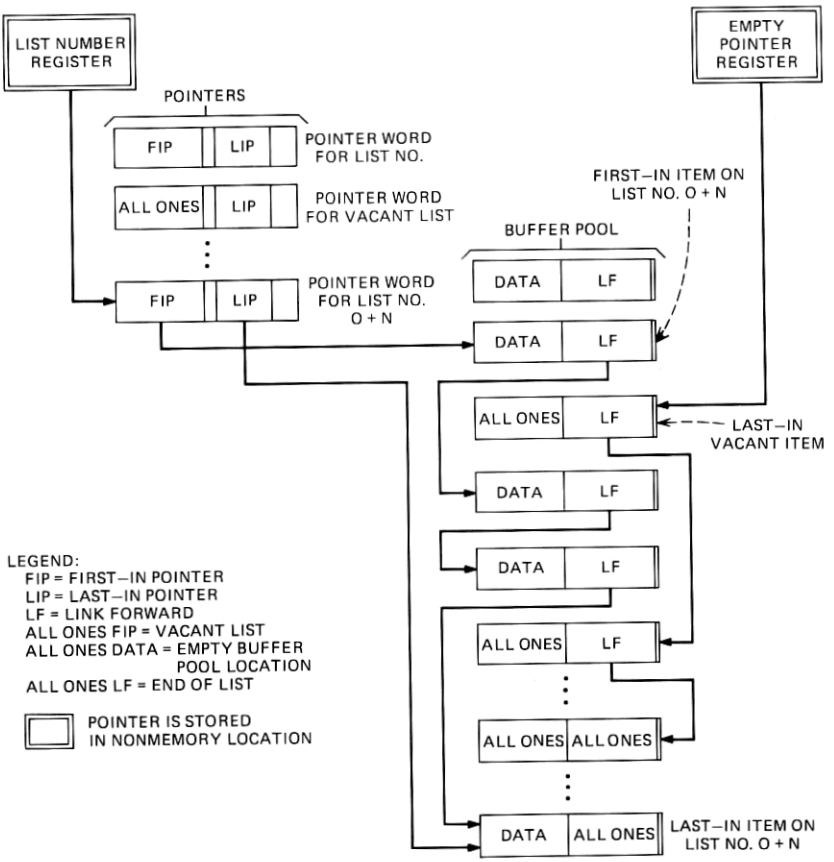

Fig. 16—List linkages.

tively. The items on a given list, not necessarily occupying sequential memory locations, are linked to one another through the use of link forward pointers stored with each item. Data memory locations in the buffer area are dynamically allocated to a specific list on an as-needed basis. Unused buffer locations are linked together on a "last-in, first-out" linked-list, referred to as the empty list. Figure 16 provides a simplified overview of these list linkages.

Decoding and sequencing of input/output operations are handled by the IOC in a four phase sequence. The remaining I/O operation, controlled by the terminal's program, is the serializing of data to and from the modem. The modem transmit and receive clocks set flags which are tested by the internal stored program. Servicing the transmit and receive flags must occur within one bit time of the modem clocks to avoid an overflow condition.

Data transmission is accomplished utilizing the 201D modem, a synchronous unit capable of data transmission at 2400 bits per second (bps) over 3002-type or equivalent, 4-wire lines. A 4-level Phase Shift Keying (PSK) modulation scheme is used. Although similar to the 201B and 201C modems, the 201D is designed to be mounted directly on the terminal unit and to be diagnosed by the processor via the TAC and terminal units.

Several overlapping techniques are employed within the terminal unit to detect faults. The primary means, which tests approximately 60 percent of the terminal's circuitry (excluding memory), is an internal self test exercise. This exercise is run whenever the terminal's signal unit processing software is idle. Supplementing these tests are hardware parity checks, a program memory sequence coding check, and a basic sanity test provided by the servicing of receive and transmit flags set by the modem. Upon detection of a fault, a particular bit is set, depending upon the failing test, in a register dedicated to recording errors for interrogation by the processor.

3.2 No. 4 ESS terminal group

Although the Central Control (CC) of the No. 4 ESS[4] System differs from the SPC No. 1A employed in No. 4A, the terminal frame designs for the two systems are functionally the same and physically similar. The terminal unit design described in Section 3.1 is common to the two systems. Peripheral bus requirements for the No. 4 ESS CC, however, dictate a terminal access controller (CONTR) design somewhat different from that of the No. 4A TAC.

The No. 4 ESS CCIS terminal group is comprised of three frames, arranged in a similar physical configuration to the No. 4A terminal group previously described. As shown in Fig. 17, the basic terminal frame accommodates up to six terminal units, duplicated peripheral bus interface (IPUB) and terminal access controller (CONTR) units along with their associated fusing, power converters, power control, and voice frequency link level adjustment equipment. Adjustment of the voice frequency link transmit and receive signal levels is achieved through attenuator and amplifier modules associated with each terminal-modem, rather than with external voice frequency link access circuits. Terminal growth beyond the basic frame is accomplished with up to two supplementary frames, each of which mounts up to 5 terminal units.

Like all peripheral units in No. 4 ESS, the CONTR employs coded enabling to respond to a CC order. With coded enabling, each peripheral has a unique name and monitors the peripheral unit bus at all times. When an order is sent over the peripheral unit bus, only that unit whose name matches the name accompanying the order responds. The name,

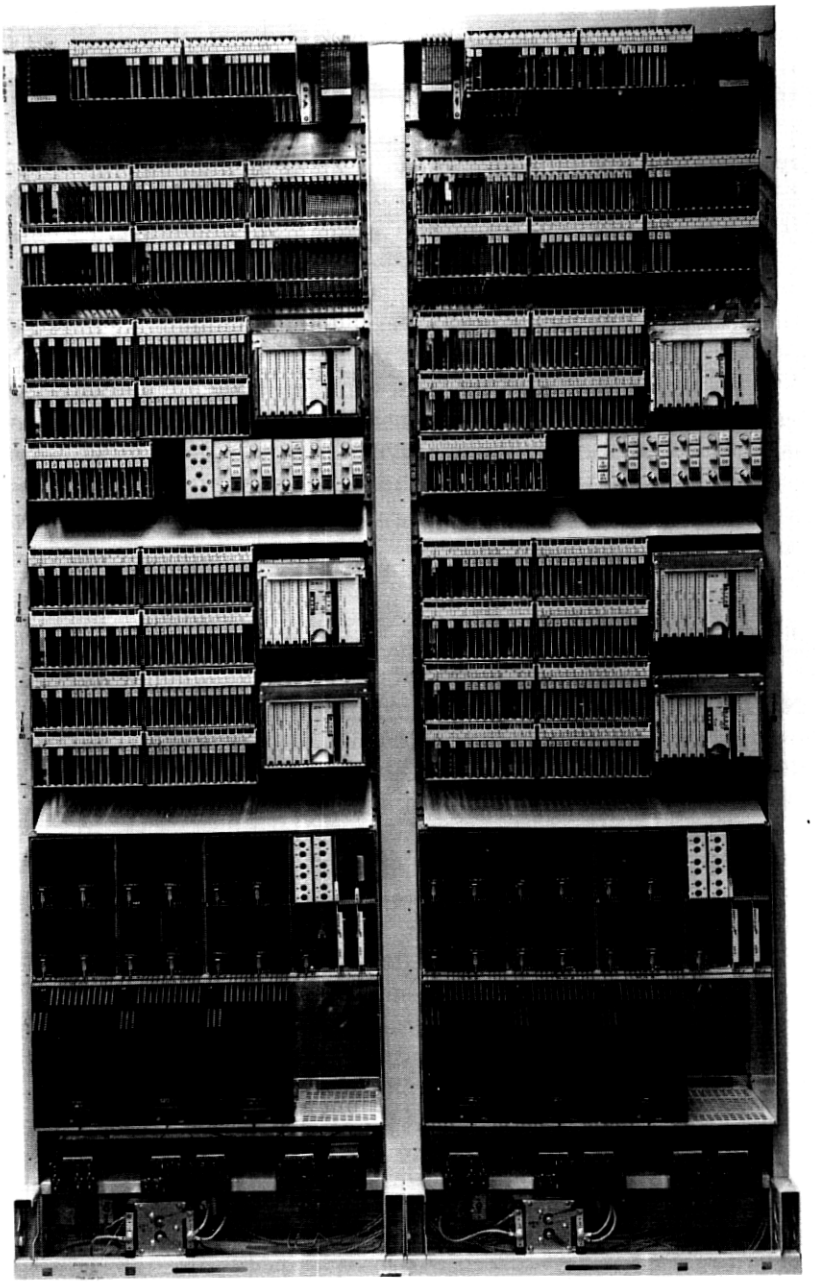

Fig. 17—No. 4 ESS basic terminal frame.

called the K-code, is sent to the CONTR on the Peripheral Unit Enable Address (PUEA) bus, the order containing the operation code, data, and optional terminal number is sent on the Peripheral Unit Write Bus (PUWB), and the CONTR replies on the Peripheral Unit Reply Bus (PURB).

Each CONTR and its mate share a common set of cable drivers and receivers contained in the IPUB units. These units allow either CONTR to be accessed from either bus 0 or bus 1. Both IPUB units are powered from a source independent of the CONTRs.

The sequence of CONTR operations is driven by a 12.5 MHz oscillator, which generates 64 decoded clock pulses, each of 80-nanosecond duration. Initiating the sequence is a synchronization pulse from the CC that precedes the K-code and data. At the beginning of each sequence the K-code is compared with the hard wired code of the CONTR, and if a match occurs, the sequence continues. If no match occurs, the sequencer is initialized and awaits the next synchronization pulse from the CC.

Sequences that follow the activation of the proper CONTR either access a terminal unit or perform the maintenance or control operations internal to the CONTR.

3.3 No. 1 ESS terminal group

The most recent addition to the family of CCIS terminal frames is the No. 1 ESS[5] data terminal group. Since this equipment is intended to be used in a more general data terminal application as well as in CCIS, its design reflects the requirements of both systems and represents a cost-effective solution to the data terminal need.

Basically the terminal group interfaces to the No. 1 ESS Processor Peripheral Unit Address Bus (PUAB) and Scanner Answer Bus (SCAB) and is enabled by the Central Pulse Distributor (CPD). Duplicated terminal access controllers (CONT) are provided which communicate with 16 terminal units. The No. 1 ESS bus system and enabling scheme is similar to that of the No. 4A System, hence the CONT and TAC unit designs are similar. Each of the 16 terminal units can be equipped with up to two modems. Only one modem is equipped in the CCIS application, however. The modem outputs are connected to the Voice Frequency Links (VFL) via Voice Frequency Link Access (VFLA) circuits which provide maintenance access to the link from an office test frame and provide a loopback path for terminal-modem fault diagnosis. A block diagram of the processor to VFL interconnections is shown in Fig. 18.

The No. 1 ESS data terminal group consists of a basic frame and two supplementary frames. The basic frame mounts duplicated CONT units and a maximum of eight data terminal units, along with two power control units and VFLA circuits associated with each terminal.

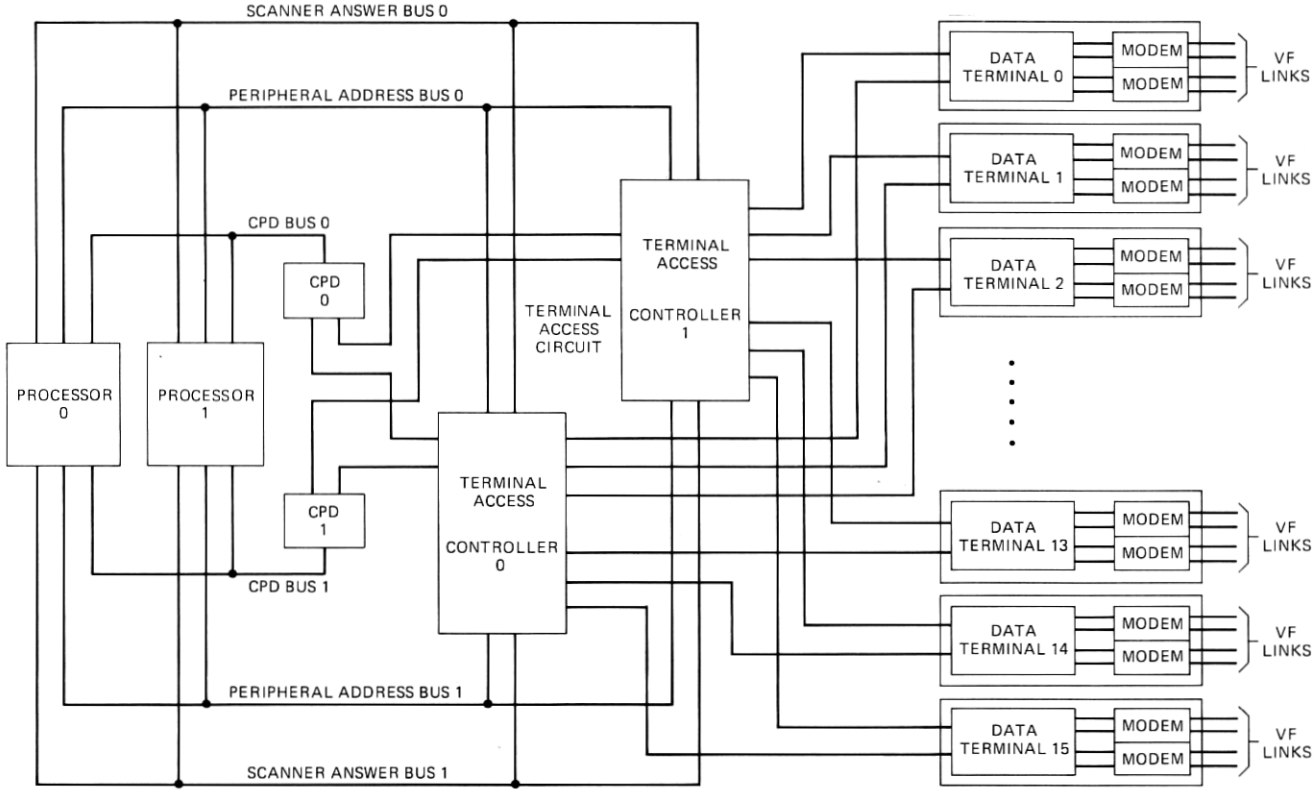

Fig. 18—No. 1 ESS terminal group block diagram.

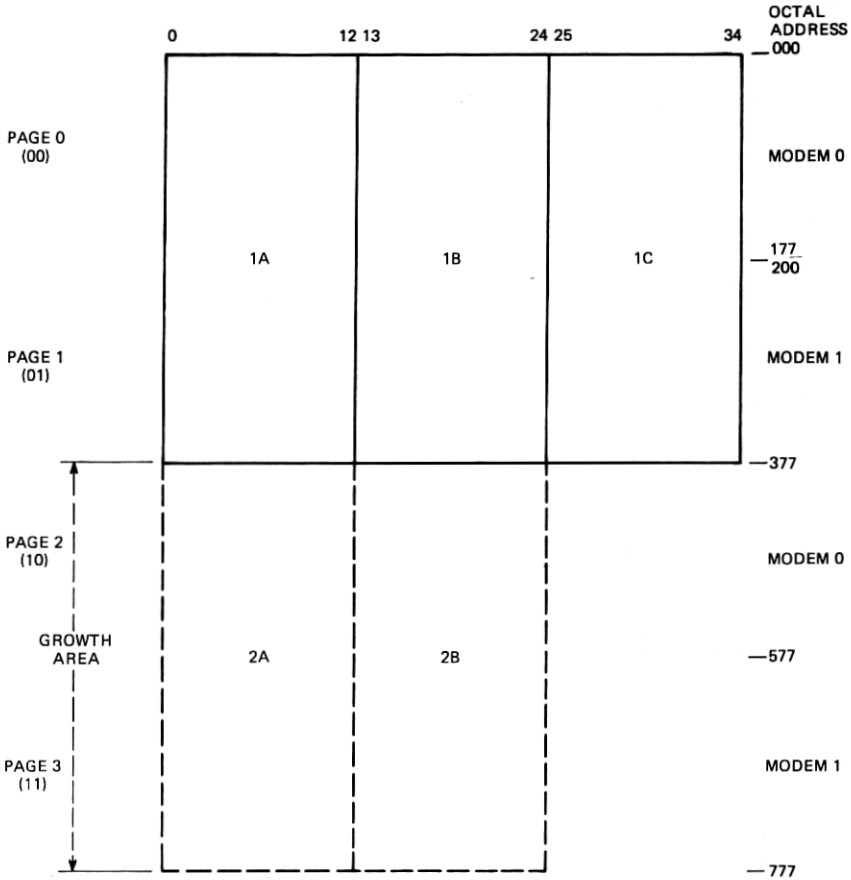

Fig. 19—No. 1 ESS terminal unit data memory organization.

Basic terminal unit architecture is retained in the No. 1 ESS design. Departures from the common No. 4 ESS design are in memory implementation and modem interfacing. The former involves the use of bipolar memory planes, each of which provides storage for 256 twelve-bit words. The resultant data memory organization is shown in Fig. 19. Alternate blocks of 128 words are assigned to each modem. Maintenance access to the VFL from an office test position is provided by the VFLA unit. The modem output can be connected to the VFL or looped back for maintenance purposes. Switched access to the VFL from a test position via the No. 1 ESS Trunk Link Network (TLN) is also allowed for initial alignment and periodic maintenance.

IV. 4A TOLL DISTRIBUTOR AND SCANNER

4.1 Introduction

The Distributor and Scanner (DAS) is a peripheral unit of the Stored Program Controller (SPC) providing autonomous base level scanning and distributing functions which are new and crucial to CCIS in the No. 4A toll application. It is primarily used to interface CCIS trunk circuits with the SPC. Each DAS frame contains 2048 distribute points and 2048 scan points. With connectorized access to the SPC Peripheral Bus System up to nine DAS frames can be provided in a 4A toll office. Each office requires at least two frames for reliability. They control up to 1700 trunks and miscellaneous points. Each additional DAS frame controls up to 2000 trunks. The distribute point is a mercury relay controlled by a flip-flop. The flip-flop is set and checked in one SPC cycle thus allowing a DAS distribute order to be executed in base level programs.

Many fault recognition and diagnostic features are part of the DAS design. Checks are made on each autonomous scan and each directed operation. When a check fails it is stored and an All Seems Well (ASW) failure is sent to the processor. A bit per point and per operation called a pest bit is provided allowing diagnostic and repair work to proceed without continual failure indications. The per point matrix pest also allows partial equipping of the matrix in groups of 512 points.

4.2 General description

A functional block diagram of DAS is shown in Fig. 20. It consists of duplicated controllers and bus access circuits and a simplex matrix. The bus I/O circuits contain the connectorized cable transformers for receiving data from the Peripheral Unit Bus (PUB) and the enable pulses. They also provide connectorized access to drive the Scanner Answer Bus (SCAB) leads and terminal strips for the various scan and distribute points used to control the frame.

The two controllers provide completely duplicated autonomous, directed and maintenance functions. During normal autonomous scanning operation they run in synchronism with matching to detect faulty operation. Most directed operations are also done in synchronism.

The matrix consists of 128 rows with each row containing 16 scan points and 16 distribute points. Access is duplicated down to the circuit packs containing the scan and distribute points.

4.3 Physical design

The Distributor and Scanner frame, Fig. 21, is a conventional ESS double bay frame. The frame is provided fully cabled to a total of 8 matrix unit (256 scan and 256 distribute points each) and is equipped

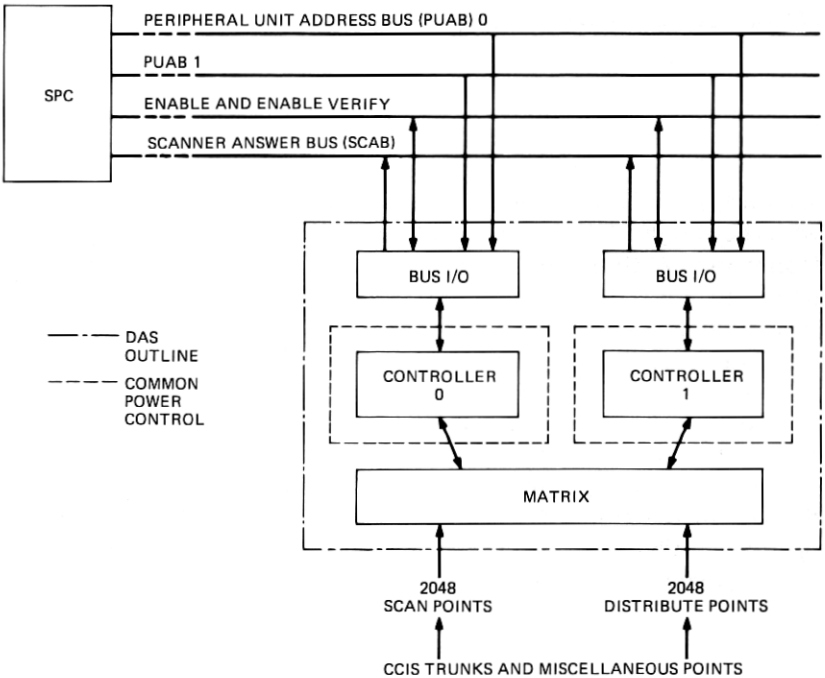

Fig. 20—DAS functional block diagram.

initially with the circuit packs for two matrix units. Growth for other than the first two DAS frames, which must be fully equipped, is to be provided with matrix packs as required for particular installations.

A fully equipped DAS frame requires 362 circuit packs of twenty different codes. The logic family used is the Western Electric Company TTL logic mounted in dual-in-line packages.

Power requirements for the frames' TTL logic are supplied via four dc-dc converters which supply the eight matrix units and two converters which are dedicated to the duplex controllers.

4.4 Matrix

The basic element in the matrix is a pair of circuit packs: the matrix point pack containing 16 distribute flip-flops and 16 scan points and the matrix relay pack containing the 16 mercury relays used as the distribute drivers. The pair is arranged in eight rows with two points per row.

Sixteen of these circuit pack pairs are arranged to make a unit of 32 rows with 8 points/row. The full matrix then consists of eight units in a 128 row by 16 points/row array.

A typical distribute and scan circuit is shown in Fig. 22. For distribute

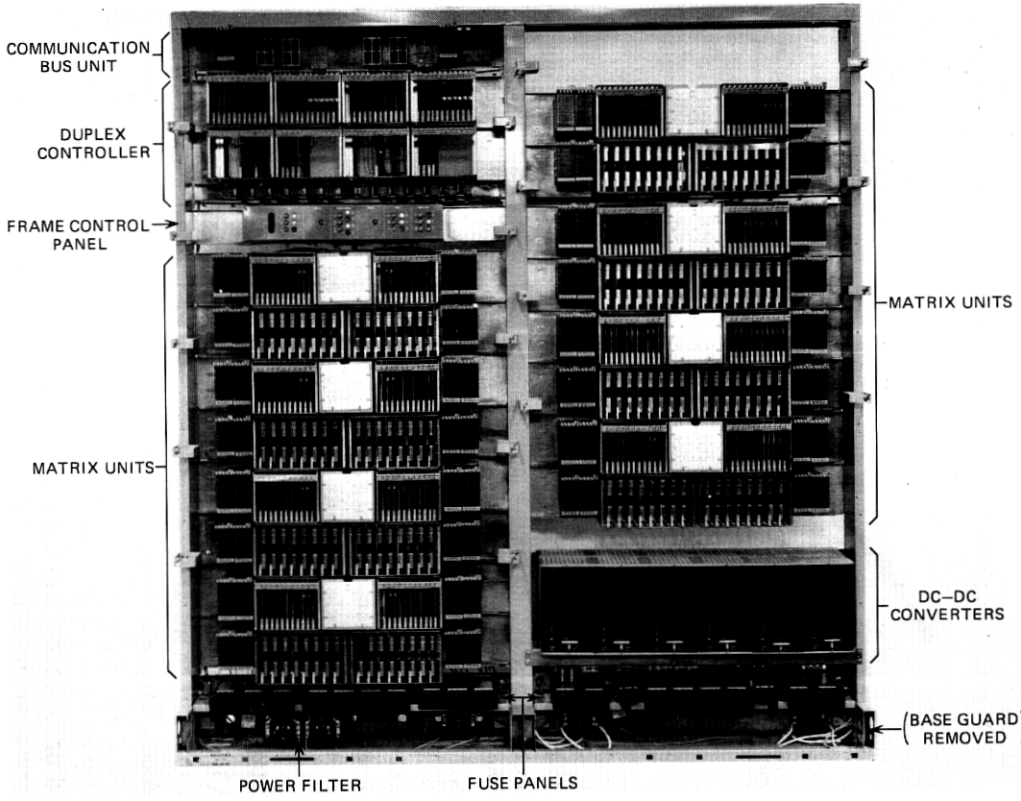

Fig. 21—Distributor and scanner frame.

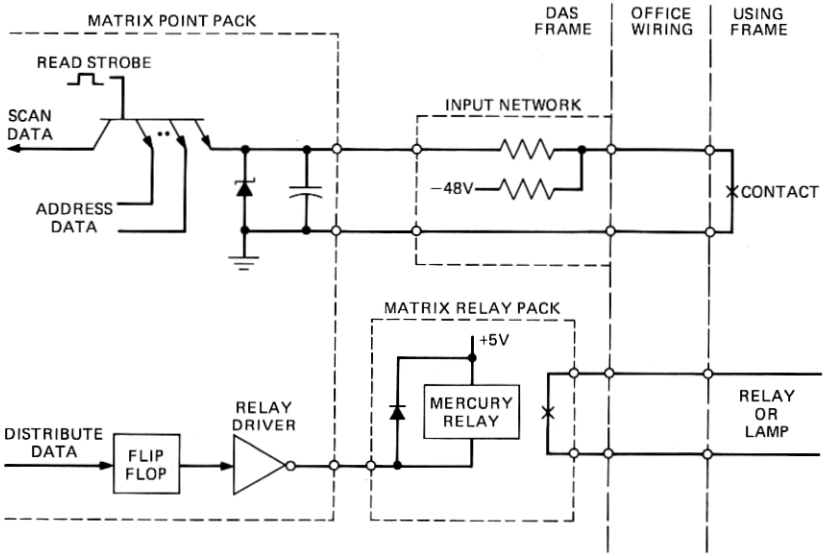

Fig. 22—Distribute and scan circuits.

a flip-flop stores the data and a relay driver is used to buffer its output to a mercury wetted relay.

The scan point consists of a resistor capacitor network which is read by a TTL gate. When the contact is closed the gate input is above 2.81 volts. In the contact open state the gate input is about 0.5 volts negative. Worst case DC noise margins at the contact are 3.8 volts when the contact is closed and 11 volts when it is open. The filter network has a delay time of 1.7 ms open to closed and 1.5 ms closed to open.

4.5 Controller

A block diagram of the DAS controller is shown in Fig. 23. It consists of a memory, a number of registers, change logic and a wired logic sequencer. The sequencer controls all operations of the controller. Normally it autonomously scans every row of the matrix, detecting and buffering any changes. When the SPC initiates a directed operation by sending an enable and data the sequencer returns an enable verify, interprets the desired operation from the data, interrupts autonomous operation, executes the directed operation, and resumes autonomous operation.

The memory is 1024 row by 18 bits/row static random access memory. Each row consists of 16 data bits and two parity bits, one over each half of the data. Memory is divided into 8 sectors, each sector having 128 contiguous rows of data. Five of these sectors (last report, last look,

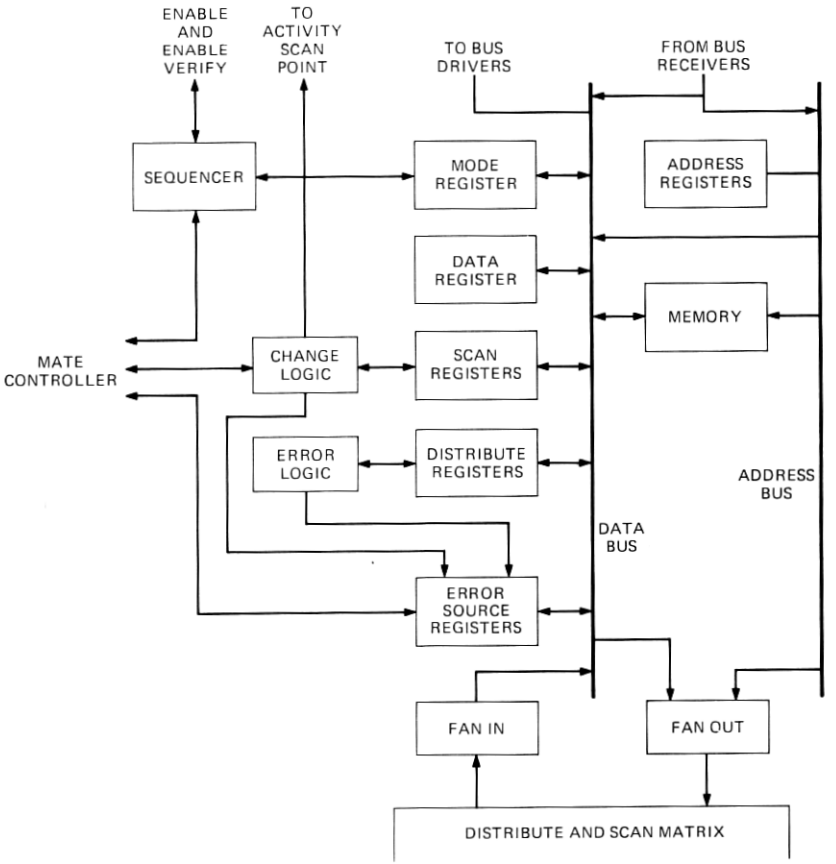

Fig. 23—Controller block diagram.

distribute memory, ignore, and pest) are direct images of the 128 × 16 matrix and are used to store data pertaining to each point in the matrix. The change buffer sector stores a word of data for each scan change detected during autonomous operation. This word contains the 12 bit address of the changed scan point and a change direction bit. Two sectors are unused.

The distribute registers, scan registers and change logic shown in Fig. 23 are used during autonomous scanning. Each register is a 16 bit parallel in, parallel out shift register. The scan registers store data on one scan row at a time. They are loaded in parallel from memory (last report, last look, ignore, pest) and from the matrix. After they are all loaded with data pertaining to the same row, they are shifted a bit at a time into the change logic. In this way the change logic processes one point at a time. If the ignore or pest bits are set, no changes are reported. Otherwise the

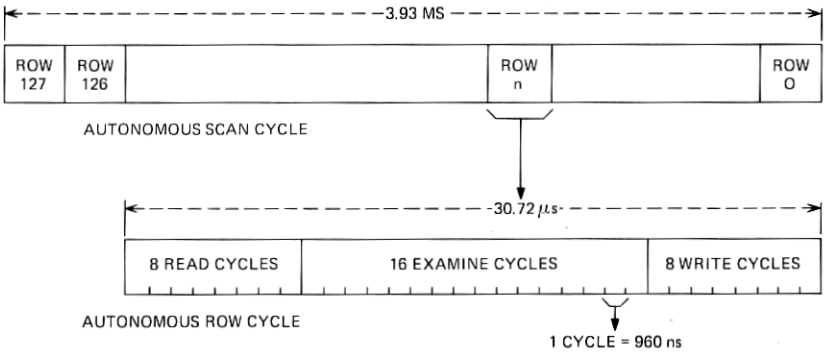

Fig. 24—Autonomous cycle timing.

change logic combines the present look at the scan point, the last look, the last reported state of the scan point and state change data from the mate controller. The result of this combination is new last report data, a change indication to the mate and a change indication for loading its own change buffer.

The distribute registers are used for trouble detection. On each matrix read operation, the state of the distribute flip flops for that row is read into one distribute register and its image read into the other. They are shifted to the error logic and compared one bit at a time. A mismatch causes an ASW failure and halts autonomous operation. This procedure checks all the access and readout circuits on a continual basis.

The mode register is a 11 bit register which controls normal and diagnostic operation of each controller. It is set by a special maintenance instruction. Bits are provided to control both normal and diagnostic operation.

4.6 Operation

The DAS has two modes of operation, autonomous and directed. Fig. 24 shows the timing of the 3.93 microsecond autonomous scan cycle of all 128 rows. For each row there are eight load cycles which load the scan and distribute shift registers from the matrix and from the memory. Then there are 16 examine cycles, one for each point in the row. During each examine cycle the change and error logic combine the data for that point. Finally there are eight write cycles during which the last report and last look memory is written and the row address counter is advanced.

There are 15 directed operations; five reads, eight writes and a autonomous scan start/stop pair. For call processing an interrogate operation returns the address and direction of oldest change in the buffer and a bit indicating if the buffer is not empty. There is also a matrix read which

returns the status of all scan (or distribute) points in a row. Four writes allow distributes to a point, a quarter row (four bits), a half row (8 bits) or a complete row. The remaining reads and writes allow the processor to read and write the DAS registers and memory for maintenance.

V. IGFET STORE

Memory for storing CCIS programs and data is provided by a semiconductor store unit using Insulated Gate Field Effect Transistor (IGFET) memory devices. A store frame (Fig. 25) consists of a controller and from one to six memory modules, each having a capacity of 32,768 words by 47 bits. The controller provides external interfaces for its memory modules and generates necessary timing and control signals. Three memory modules are required in a CCIS switching office, and one memory module is needed in a CCIS signal transfer point. Store frames are duplicated for reliability.

The IGFET memory device is 4096 words by one bit, using n-channel technology. The device is dynamic, with refresh provided autonomously by the store controller. Sixteen memory devices are packaged on a memory plane containing 32,768 words by two bits. A memory module consists of 24 memory planes with the controller. Five-volt Transistor-Transistor Logic (TTL) devices are used in the nonmemory portions of the store.

VI. OUTPULSER FRAME

On all incoming CCIS calls served by new trunks, an outpulser must be connected to permit the marker to establish the cross office connection. The outpulser also provides access to circuitry which tests continuity of the CCIS transmission facility. In the case where a conventional outgoing trunk is selected, the outpulser transmits the address digits to the next office.

The outpulser unit is a modified Multi-Frequency (MF) sender with the MF receiver unit and incoming digit registration circuitry removed. The modification also adds the ability to connect to the circuit which tests CCIS trunk continuity and the ability to receive address digit loads from the processor.

Three outpulser units are mounted on an outpulser frame (Fig. 26). These are arranged into groups with up to 48 outpulsers per group. Up to three outpulser groups can be provided per office.

VII. CCIS OUTPULSER LINK—TRUNK COMPLEX

An equipment module consisting of three CCIS trunk frames and one outpulser link frame is designed as a fully connectorized module. This design permits the factory to prepare all cabling between the four frames

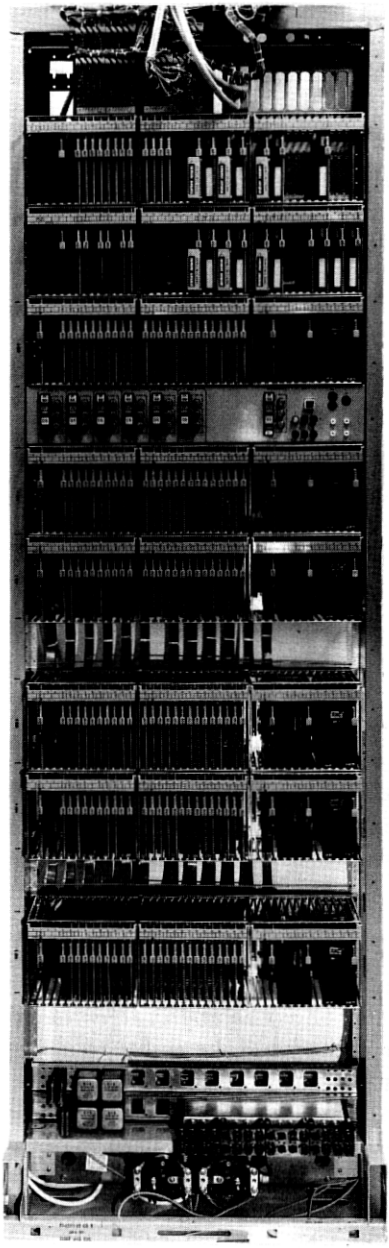

Fig. 25—IGFET store frame.

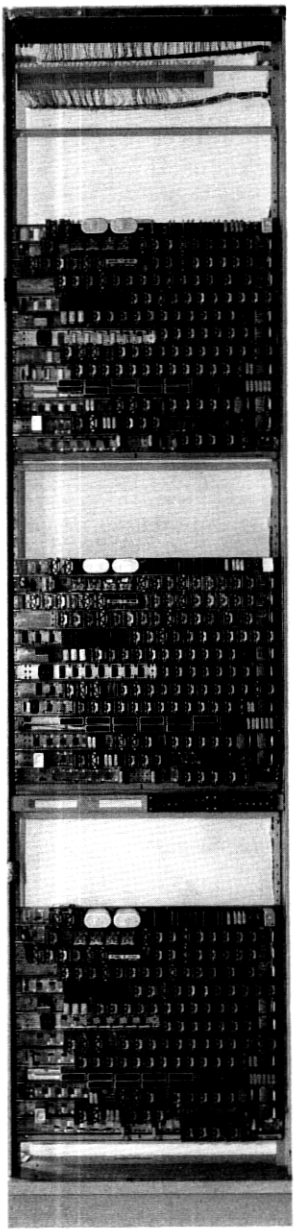

Fig. 26—Outpulser frame.

in module. A total of 360 trunks are attached to their respective outpulser link appearance by connectorized umbilical cables provided on the trunk frames and mated with frame connectors on the link frame at the time of installation. In addition the cabling between 11 outpulser link frames, which form a group, are connectorized. These link frame cables provide the ability for all trunks to access every outpulser in the associated outpulser group. This permits easy rearrangement during growth additions as well as ease of connection during initial installation.

7.1 Outpulser Link Frame

The outpulser link consists essentially of small crossbar switches and functions to connect an incoming CCIS call to an outpulser. The frame, Fig. 27, contains three links, one for each of the associated trunk frames in the module. Each trunk on a link has access to every outpulser in its outpulser group through the connection in the outpulser link.

7.2 CCIS Trunk Frame

The CCIS trunk frame accommodates a total of 120 plug-in trunk units. The trunks consist of epoxy coated steel boards making use of miniature wire spring relays and other low profile components. A typical trunk is shown in Fig. 28. Use of the metal boards takes advantage of the structural and thermal characteristics of these substrates. The connectors for the plug-in trunks are hard wired at the trunk frame to cables which are connectorized at the outpulser link. A test housing, to be equipped in every third trunk frame, provides a convenient station for the manual testing of any of the trunks in the same frame or adjacent frames.

7.3 Outpulser Link Controller Frame

An outpulser link controller frame, Fig. 29, provides the necessary logic to operate the outpulser link when an incoming CCIS call is connected to an outpulser. As part of this operation the controller also passes the identity of the trunk and outpulser to the SPC. In addition the outpulser link controller functions to connect a transceiver to the outpulser when requested by the processor. A single outpulser link controller frame is required for each outpulser group. Each frame provides four controller units to serve the associated outpulser group.

VIII. TRANSCEIVER AND CONNECTOR FRAME

The transceiver and connector frame, Fig. 30, provides the ability to test the voice path when the associated signaling is carried over the CCIS data link. The transceiver generates tones and has a receiver for verifying the integrity of the talking path under test. The connector portion of the

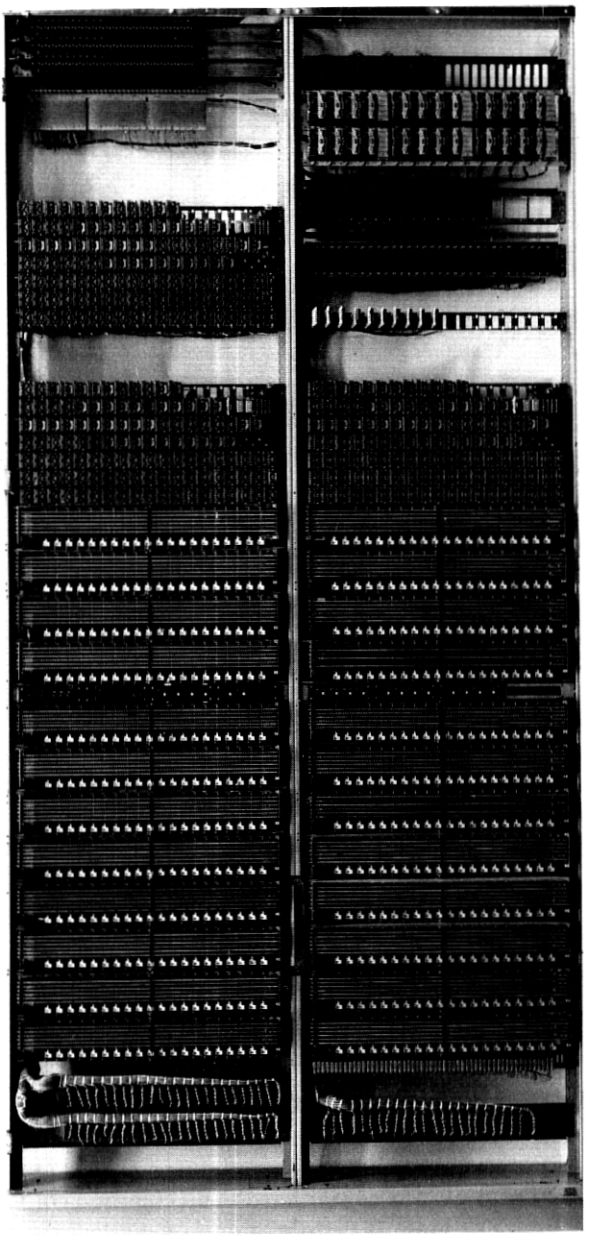

Fig. 27—Outpulser link frame.

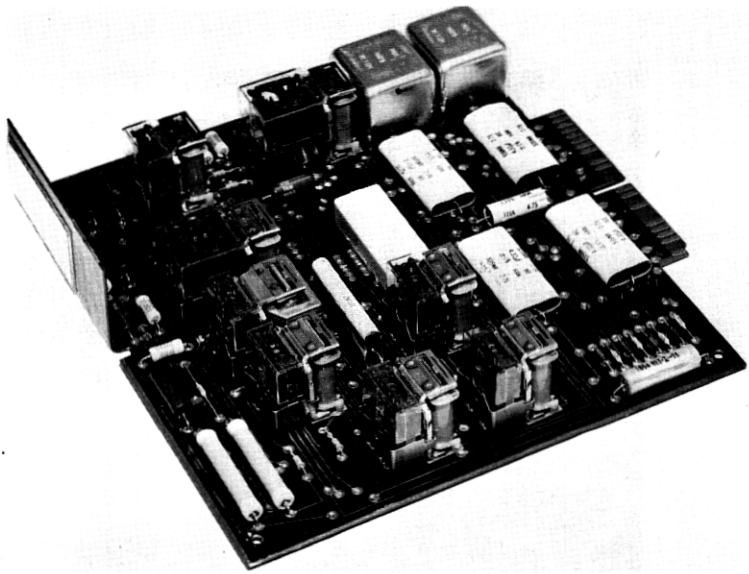

Fig. 28—CCIS plug-in trunk.

frame uses connectorized patch cables to provide multiple appearances of the transceivers which enhance rearrangements during growth.

IX. AUXILIARY DECODER CONNECTOR

The Auxiliary Decoder Connector (ADC), Fig. 31, is provided to increase the capacity of each connector of the basic Decoder Connector (DC). The additional leads provided increase the number of address digits which the DC can handle. These additional digits permit the entire address to be read from the sender or loaded into the outpulser for transmission to the next office.

X. MODIFIED EQUIPMENT

10.1 Options and planning

Most 4A crossbar and ETS circuits require some alteration, either minor or substantial, to operate with CCIS. The majority of the CCIS market in 4A crossbar will be in conversions of existing machines. CCIS features are now provided as standard in all common control circuits so that all subsequent manufacture of common control hardware will be CCIS compatible.

Circuits such as trunks, ETS, Peripheral Bus Computer (PBC) and test frames introduce the CCIS changes as options.

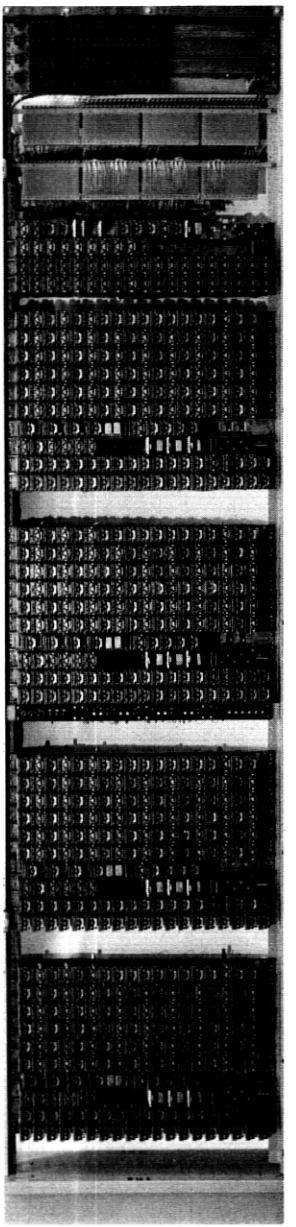

Fig. 29—Outpulser link controller frame.

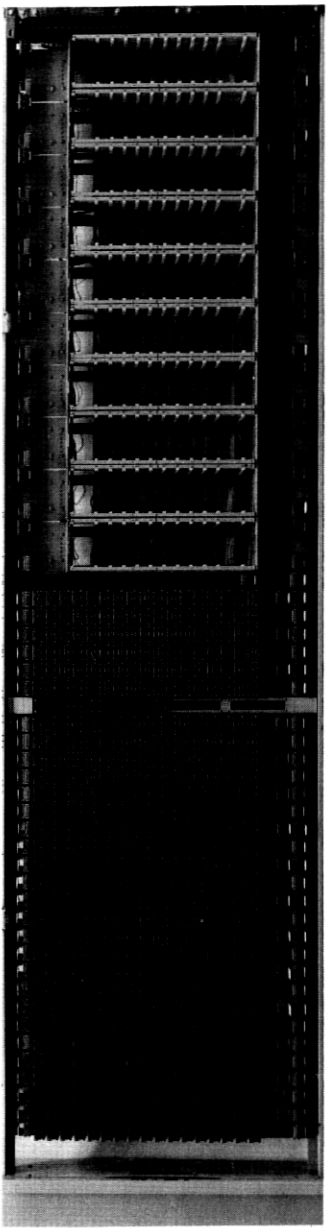

Fig. 30—Transceiver and connector frame.

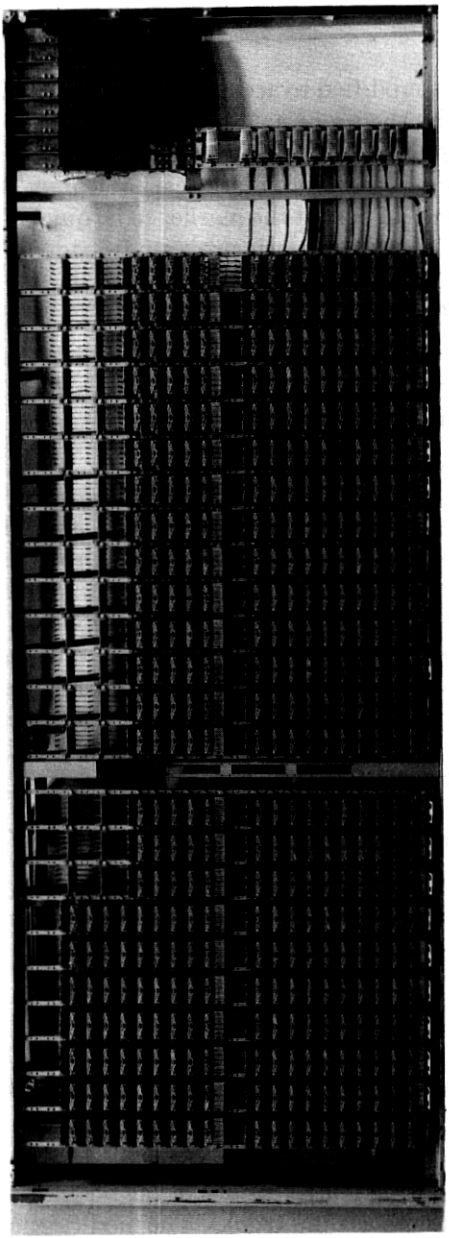

Fig. 31—Auxiliary decoder connector frame.

This permits the customer to acquire the CCIS features only where required.

10.2 Marker

The marker is modified to accept the outgoing link address of a CCIS trunk selected by the processor and to establish a connection between a sender or outpulser and the transceiver. This circuitry is contained in a single unit, added to the standard marker frame. The unit contains a cross connect field to permit the marker to be quickly converted to CCIS operation after the CCIS generic program is loaded.

10.3 Outgoing link frames

Relays are added to this frame through which the marker can seize a CCIS trunk previously selected by the processor. This change is contained in two units per link frame.

10.4 Senders

Senders are modified for CCIS to provide all address digits to the processor. This change is required so that the processor can transmit the entire address field to the next office when an outgoing CCIS trunk is selected. In addition the MF sender must be modified to serve also as an outpulser when the trunks served contain both conventional and CCIS trunks. This requires the capability of accepting the address digits to be outpulsed from the processor via the decoder channel. These changes are accomplished by adding relays to the existing units plus some associated wiring changes.

10.5 Decoder channel

The decoder channel is modified to permit handling all eleven address digits of a call. This change is accomplished by addition of apparatus into existing space on the unit.

10.6 Decoder connector

CCIS requires only wiring changes to associate the Decoder Connector (DC) with the auxiliary DC to increase its data capacity.

10.7 EM trunks

Standard mounting plate versions of the MF intertoll trunks may be field modified for use as CCIS trunks. The modification opens the E&M leads, provides for looping the transmit and receive speech pairs for voice path assurance testing, adds connections to the Distributor and Scanner (DAS) for supervision and control and provides a connector for patching

the facility side of the trunk for transmission tests. The modification includes a rotary switch control to permit either MF or CCIS operation.

10.8 Electronic Translator System and Peripheral Bus Computer

Minor changes are required on the Alarm and Display (A&D) and Teletypewriter Buffer (TTYB) frames. The A&D is changed to add lamps and logic associated with new CCIS hardware. Additional TTYBs are required to serve additional teletypewriters used for CCIS.

The PBC modification requires additional core memory to accommodate the increased amount of data for CCIS traffic and an additional disk unit. The expansion requires the addition of one cabinet, some relocation of hardware units among the resulting four cabinets and associated cabling changes.

XI. NEW TEST FRAMES AND INTERFACES

11.1 Outpulser Link Controller Test Frame (OLCTF)

The OLCT frame, Fig. 32, and the CCIS Intra-Office Trunk Test Frame (CIOT) together form a small test center located in the CCIS trunk area of a 4A switching machine. The OLCT performs processor controlled scheduled operational tests of the controller and manually requested tests in conjunction with trouble clearance by the craftspersons.

A single bay contains the logic units, control panel, lamp displays and writing shelf which comprises the OLCT frame.

11.2 CCIS Intra-Office Trunk (CIOT) test frame

This test frame, Fig. 33, performs scheduled operational tests of CCIS trunks under processor control. Manual testing via a TTY associated with this test frame can also be performed to aid trouble clearing and circuit order testing. Test connections may be held to permit manual transmission measurements.

The CIOT consists of a single bay frame. A control and lamp panel, a writing shelf, relay logic units and a telephone handset are component parts of the hardware arrangement. An associated TTY is dedicated to this test frame for I/O functions. This test frame along with the outpulser link controller test frame form a remote test center.

11.3 VFL test frame

The Voice Frequency Link (VFL) test frame, Fig. 34, provides the ability to perform manual transmission tests on CCIS data links. It is intended for use only at the Signal Transfer Point (STP) locations where

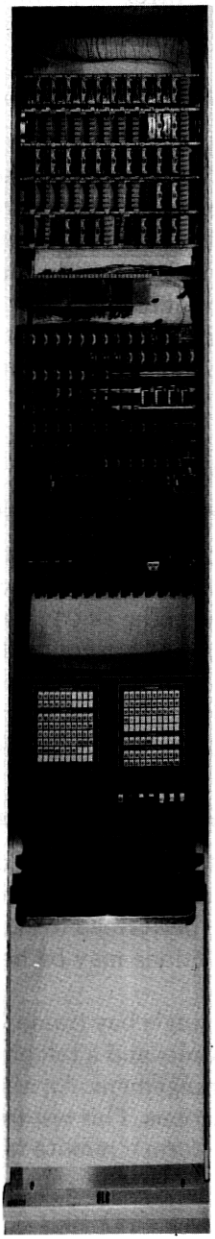

Fig. 32—Outpulser link controller test frame.

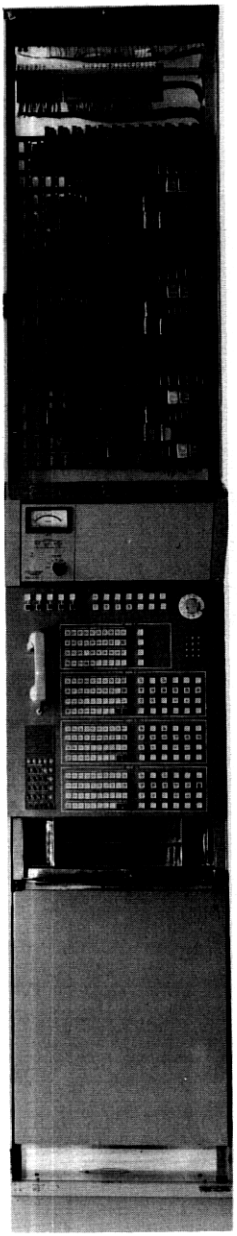

Fig. 33—CCIS intra-office trunk test frame.

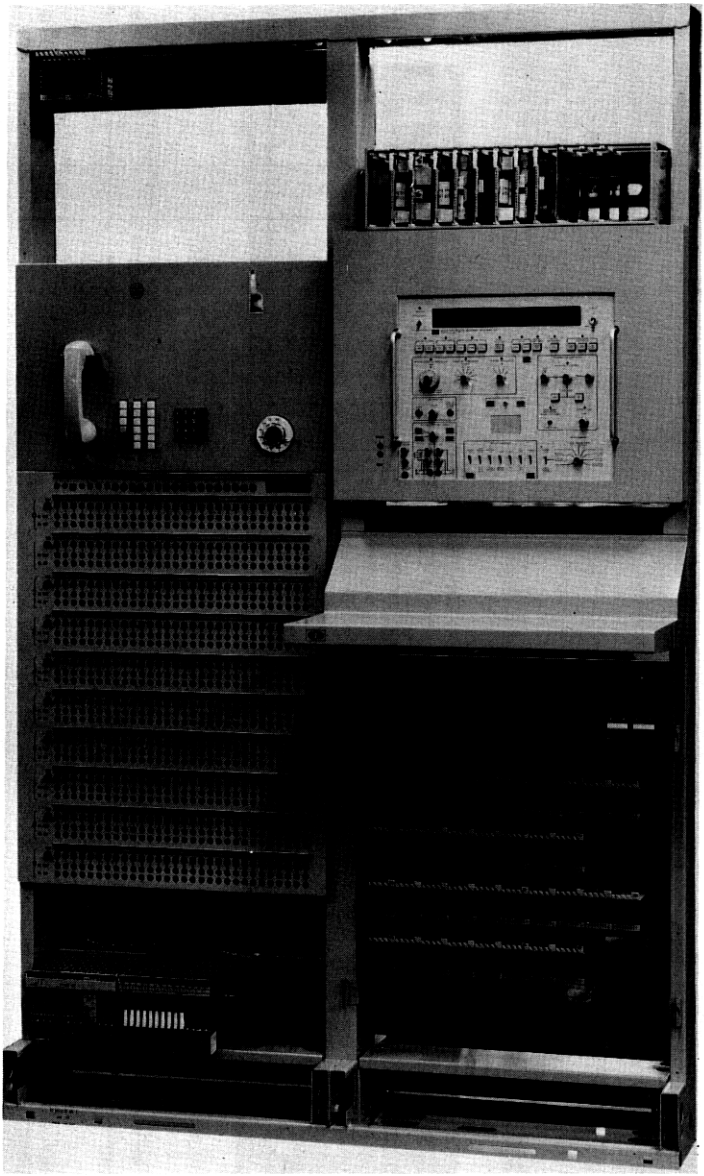

Fig. 34—Voice frequency link test frame.

there are large numbers of VFLs. The test appearance of a VFL is switched to the VFL test frame under processor control. The frame provides a Transmission Impairment Measurement (TIM) test set for manual tests. A telephone set and control logic for connecting to various communi-

cation circuits is also provided. An ETS teletypewriter (TTY) provides the I/O function.

The VFL test frame is contained on a double bay framework. Jacks are provided for 300 VFL appearances on the jack bay. A cross connect field is provided to permit regrouping the VFL appearance on the jack bay without office cabling changes.

11.4 Voice Frequency Link Access Unit and Frame

This circuit performs the switching necessary to disconnect a voice frequency link from the CCIS terminal and connect it either to the VFL test frame for manual testing or to the maintenance terminal for automatic testing. As shown in Fig. 35, eight VFL access units are provided in a single bay frame. Each unit serves four CCIS terminal units. This frame is required in an STP, but not in a CCIS switching office, where only a VFL access unit is required.

XII. MODIFIED TEST FRAMES

12.1 Trouble recorder

This frame was modified to add CCIS information to the trouble record card, to add circuitry for testing the operation of CCIS features in the 4A common control hardware and to provide additional alarm and status lamps. It was implemented by adding two new units, some components to existing units and a new trouble record card.

12.2 Incoming Sender Register Test (ISRT) frame

This test frame was modified to perform tests of the CCIS features in senders, outpulsers and sender/outpulsers. In addition the ISRT was altered to test the transceivers which are used by CCIS to test the continuity of voice paths. Output information on hard faults is sent to the maintenance TTY. These changes were incorporated by adding a new unit to the frame plus some component changes on the frame control panel.

12.3 Automatically Directed Outgoing Intertoll Test (ADOIT) frame

The ADOIT frame was modified to perform automatic transmission testing of CCIS trunks. The test connector is not used by the ADOIT to access CCIS trunks; instead ADOIT to processor communication is used to request the processor to reserve the designated trunk for the ADOIT connection. The changes were accomplished by addition of apparatus and wiring to existing units on the ADOIT frame.

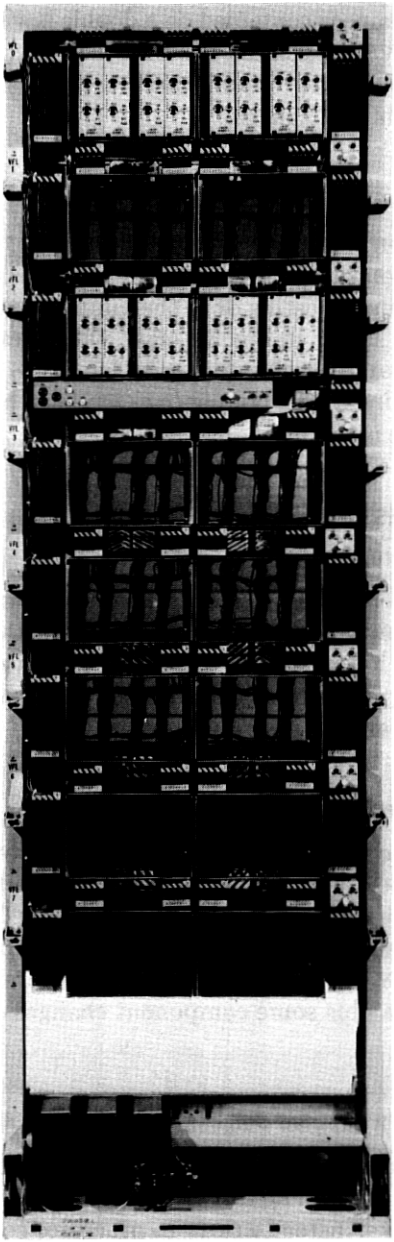

Fig. 35—Voice frequency link access frame.

XIII. TRANSMISSION EQUIPMENT

13.1 Integrated Manual Test Frame (IMTF)

This frame provides for the manual testing of both conventional and CCIS trunks. The frame has two test access appearances on the switching machine and can optionally be equipped for Switched Maintenance System 3B (SMAS) which can gain access to points in the transmission terminal equipment. This arrangement allows the cross office testing to be performed by one person. The test portion of the IMTF is shown in Fig. 36.

For CCIS trunk testing access is made via the Teletype Corporation *DATASPEED* 40 teletypewriter. The *DATASPEED* 40 interfaces the SPC through the Teletypewriter Buffer (TTYB) and can be used by the craftsperson to access a specific trunk, control the state of certain equipments, and to obtain information from other test frames.

Each test access via the switching machine is monitored during the call setup. Certain operational problems which halt call progress are displayed as an aid in trouble isolation. Transmission level and noise measurements can be made from test lines or with a craftsperson in the distant office.

The IMTF is optionally provided with a return loss measuring set and/or an echo suppressor measuring system depending on the assignments of toll connecting and intertoll trunk testing. Jacks are provided for the use of portable equipment.

The Voice Frequency Links (VFL) for the switching offices appear in the Test Trunk and VF Link Jack (TTJ) bay which is adjacent to an IMTF. The test appearance of the VFL is switched to the TTJ bay by the processor. From there it can be patched to the IMTF for transmission measurements. Portable test equipment can be used if required, such as for envelope delay distortion measurements. The TTJ also provides test trunks and lines to other test frames and equipment.

The IMTF has been arranged to group together those functions which are needed to permit one person to isolate trunk and facility problems. The IMTF is part of what is known as a Trunk Operations Center (TOC), which is responsible for pre-cutover and circuit order testing. The general trunk maintenance functions include trouble detection, service protection, sectionalization, verification, and others.

To support these functions SPC channel 6 and PBC channel 26 are available in the TOC to present information such as trunk status.

13.2 Outgoing Trunk Testing System (OTTS)

The Outgoing Trunk Testing System (OTTS), Fig. 37 is a microprocessor centered, minicomputer controlled test frame that operates automatically to test all intertoll and toll connecting message trunks

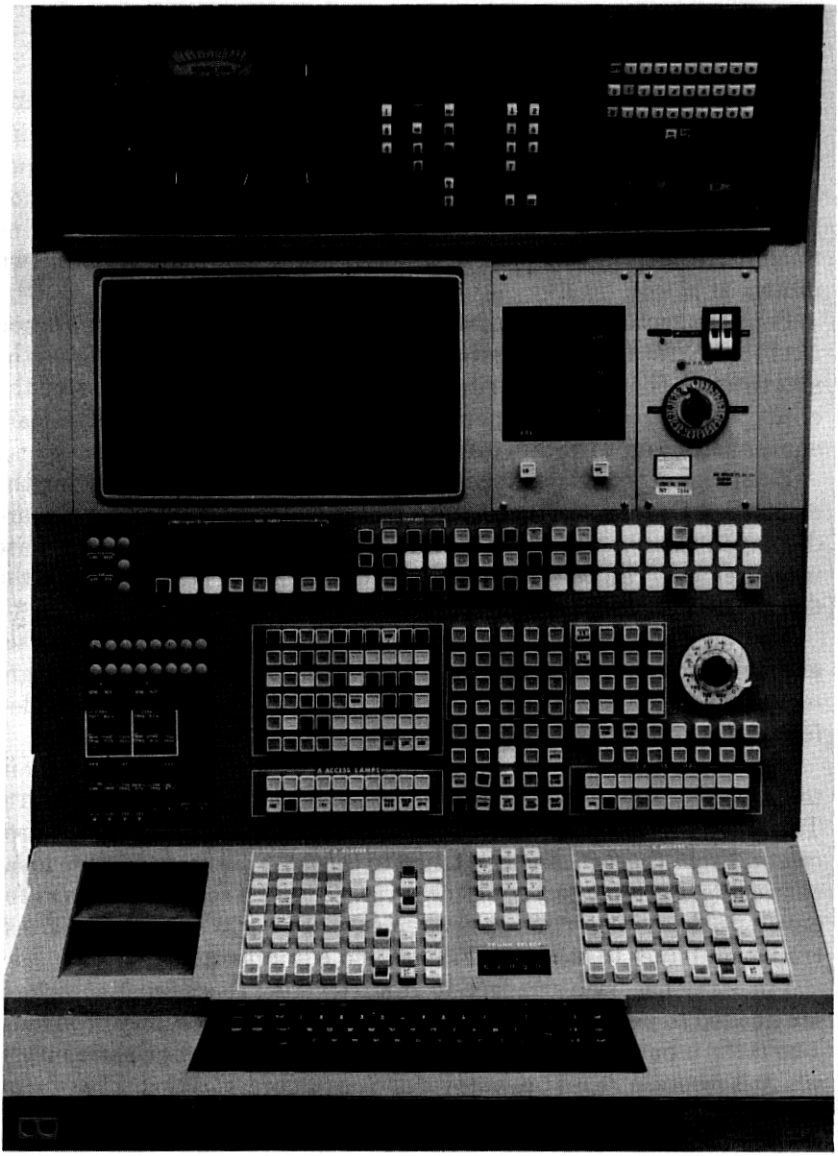

Fig. 36—Close up of integrated manual test frame.

outgoing from a No. 4A switching machine. The minicomputer providing the control can be colocated with and connected directly to the OTTS [the Trunk and Facilities Maintenance System (TFMS) configuration] or may be remote and controlled via a Direct Distance Dialing data link [the Centralized Automated Reporting on Trunks (CAROT) configura-

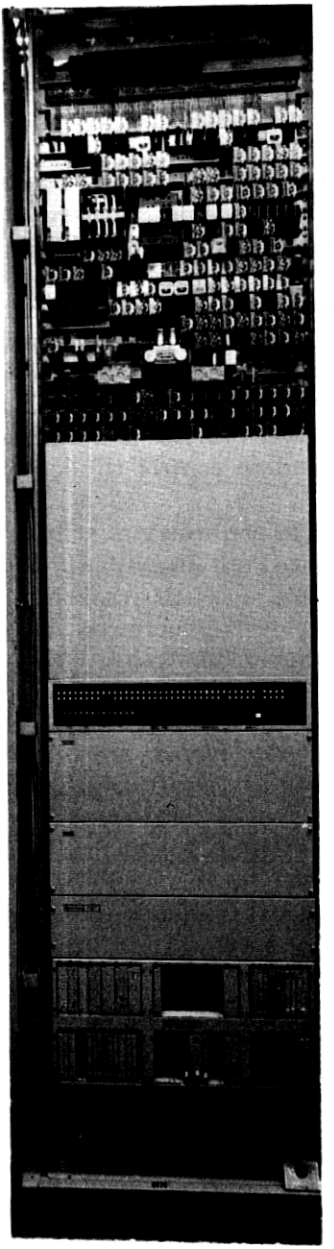

Fig. 37—Outgoing trunk testing system bay.

tion]. In either case, the minicomputer serves to specify a trunk and a test. The microprocessor part of the OTTS equipment serves to control, monitor and report the results of each test.

OTTS is able to conduct tests on two trunks simultaneously via the switching machine and results in sufficient capacity in a single test frame to complete all the trunk testing requirements of even the largest No. 4A offices.

For conventional trunks, OTTS performs tests to all standard operational and transmission test lines. Following any of these, a supplementary trunk identification, trunk verification, disconnect timing (for intertoll trunks) or incoming release (for toll completing trunks) test may be made. Alternatively, any of a variety of special abbreviated trunk tests may be specified. Preceding each test, a set of call process checks is made. Any failure terminates the sequence with a report message to the controlling minicomputer. OTTS may be controlled to complete to a busy trunk, distinguish between service and maintenance busies (without service disruption) and to control the lockout relays of equipped trunks.

For CCIS trunks, OTTS performs tests only to transmission test lines. Before each test, a Voice Path Assurance (VPA) check is made. The results of the VPA check are reported to the controlling minicomputer, but the transmission test line test is continued independent of those results. Following each transmission test a special CCIS release timing check is made.

These tests can be made on CCIS trunks made maintenance busy at the near-end. Trunks may be made maintenance busy or returned to service from a maintenance busy state. A sequence of call progress checks analogous to those for conventional trunks is made. For conventional trunks, OTTS interfaces the No. 4A switch as two incoming trunks. OTTS performs its own sender functions and interfaces with the common control via a single decoder connector appearance. OTTS identifies the trunk to be tested to the marker via the test connector and a dedicated trunk block connector.

Similarly for CCIS trunks, OTTS interfaces the switch as two incoming conventional trunks. The same decoder connector appearance is used as is used for conventional trunks to initiate the switching process, but for CCIS trunks the trunk to be seized and the call destination are identified to the switch via a pair of multi-lead interfaces with the DAS circuit of the SPC.

User interaction with OTTS in the TFMS configuration takes place via two local Trunk Maintenance teletypewriters. One terminal is customarily dedicated to tests on intertoll and the other to tests in toll connecting trunks. The TFMS configuration operates in two distinct modes, routine and demand.

In the routine mode of operation, all trunks are tested by traffic group in a predetermined sequence. Only those tests that fail are reported, and busy trunks are stored for retesting at 30-minute intervals. In the routine testing mode, CCIS and conventional trunk groups may be mixed.

In the demand mode of operation, a formatted request may be entered at a trunk maintenance terminal and cause one or more repetitions of any test sequence in the repertoire to any trunk or group. The results of any test made in the demand mode are reported, whether or not the test results are passing.

User interaction with OTTS in the CAROT configuration can take place in any of three modes, each of which requires that the OTTS be converted to a Remote Office Test Line (ROTL) by application of an optional OTTS/ROTL unit. The OTTS/ROTL unit serves to interpret communications between the CAROT processor and the OTTS sequence controller.

The routine mode for the CAROT configuration is similar to that for the TFMS configuration except in that the processor is remotely located and the output (trouble) reports are prepared on a line printer colocated with the CAROT processor. Similarly, a demand mode exists in the CAROT configuration in which the request is made from and the results are reported to a terminal connected to the CAROT processor either directly or via a direct distance dialing data link.

The third mode of interaction with OTTS consists of direct connection of a Manually Controlled Interrogator (MCI) to the OTTS/ROTL unit in the OTTS bay. Using the MCI, any test sequence in the repertoire can be made repetitively and the results are displayed on panel lights on the MCI.

13.3 Unitized terminal equipment

Modern No. 4A crossbar and No. 4 ESS toll offices utilize Unitized Facility Terminals (UFT) to provide all the termination, signaling and channel bank equipments needed for toll trunks in compact prewired packages. This UFT family has been expanded to include frames for use with CCIS trunks. Four frames sets have been added.

Two sets of frames were designed primarily to be compatible with No. 4A crossbar offices. One, a set of three frames provides a complete terminal for 480 trunks including channel banks, carrier supply and distribution, power supply and distribution, transmission level adjusting attenuators, and maintenance and communications equipment. The second frame set design adds echo suppressors to the unitized terminal. Similar frame sets were designed primarily for ESS offices in arrangements with and without echo suppressors. The frame including echo suppressors will not be needed in No. 4 ESS offices after the introduction

of the digital echo suppressor terminal but will be needed in No. 1 and No. 1A ESS offices.

The CCIS frames occupy only one-half the floor space needed for similar UFT equipment which include signaling units.

All frames are arranged for convenient in-aisle maintenance access and communications. Optionally, the frames may be equipped with plug-in maintenance connectors to provide dial-up remote access to all trunks at the carrier interface (+7, −16 TLP) from the IMTF or other test position.

In the transition to CCIS it will be desirable to utilize existing equipment arrangements at least temporarily. Plug-in units interchangeable with SF signaling units have therefore been made available. These units provide only the attenuators for transmission level adjustment.

XIV. SUMMARY

The application of CCIS to the toll network has taken advantage of existing but modern hardware technology in the various switching systems to reduce development time and cost to the network. New units and frames have been required as well as modifications to existing switching equipment. The technology matches exactly that being used in new ESS offices and has been optimized for ease of conversion of existing No. 4A crossbar offices. The design should allow rapid expansion of the CCIS network.

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